Energy-Efficient Superconductive Integrated Circuits Based on Adiabatic Quantum-Flux-Parametrons: Towards Large-Scale and High-Dense Integration

Christopher L. Ayala¹ & Nobuyuki Yoshikawa²

Yokohama National University – Institute of Advanced Sciences, Yokohama, Kanagawa, Japan

¹email: ayala-christopher-pz@ynu.ac.jp • chris.ayala@ieee.org
²email: yoshikawa-nobuyuki-gt@ynu.ac.jp
Yoshikawa Group @ YNU
Institute of Advanced Sciences (IAS)
Cyber Hardware Security Research Cluster
Extremely Energy-Efficient Processors Research Unit

Prof. Nobuyuki Yoshikawa
Prof. Thomas Ortlepp (adjunct)
Prof. Yuki Yamanashi
Prof. Christopher Ayala
Prof. Lieze Schindler
Mr. Michael Johnston
Dr. Hideo Suzuki
Prof. Naoki Takeuchi (now @ AIST)
Prof. Olivia Chen (now @ TCU)
Prof. Yuxing He (now @ SWJTU)

Dr. Ro Saito (Hitachi)
Tomoyuki Tanaka
Shohei Takagi
Yu Hoshika

Yuki Murai (Microsoft), Mae Nozoe, Takehisa Yamada (NRI), Risako Saito, Safwan Azman, and many more…

Prof. Lieze Schindler
Mr. Michael Johnston
Outline

- Introduction – motivation and background
- Challenges in AQFP logic
  - Area
  - Driving strength
  - Clocking
- Towards practical applications
- Summary
Motivation

Trend of rising electricity demand of information and communications technology (ICT).

Approaching 10% of the total electric power worldwide in 2020.

Facebook Data Center, Lulea, Sweden

Performance: 27-51 PFLOP/s
Power 84 MW avg* (120 MW max)
D.S. Holmes, ISS 2013, Tokyo, Japan.
http://worldstopdatacenters.com/renewable-energy-output-rankings/

Worst-case scenario: ICT could use as much as 50% of global electricity by 2030.


AQFP logic for computing

- **Adiabatic quantum-flux-parametron (AQFP) logic**
  - Composed of a pair of Josephson junction (JJ) superconductor devices
  - Extremely small bit energy $<< I_c \Phi_0$
    - Very small switching energy due to adiabatic operation
    - 1.4 zJ per JJ at 4.2 K in experiment [1]
  - High gain
    - 10-50x gain from μA’s of input current
  - High robustness
  - Clock speeds on par with state-of-the-art CMOS logic (5-10GHz)

After cooling overhead [2], ~80x more efficient than 7nm FinFET with $V_{DD} = 0.8V$ [3]

Adiabatic quantum-flux-parametron (AQFP)

+\( I_{\text{in}} \) → SFQ stored in left loop, logic ‘1’.
-\( I_{\text{in}} \) → SFQ stored in right loop, logic ‘0’.

Operation is based on conventional QFP gates [1].
Switching energy can be reduced below \( I_c \Phi_0 \) via adiabatic operation.

Data propagation in AQFP logic

Adiabatic switching in JSIM. Measured to be 1.4zJ/cyc. at 5 GHz [1].

Any combinational logic gates can be designed by arraying the four building blocks.

Cell library: minimalist design

L_in = 1.13 pH
L_x = 5.67 pH
L_d = 6.16 pH
L_1, L_2 = 1.53 pH
L_q = 7.88 pH
L_out = 31.9 pH
k_d1,k_d2 = -0.154
k_x1,k_x2 = -0.209
k_out = -0.515
J_1, J_2 = 50 µA

Excitation/clock lines are 50Ω microstriplines
Interconnect are shielded striplines

4-layer Nb/AlO_x/Nb 10 kA/cm² high-speed standard process (HSTP) by AIST, Tsukuba, Japan
Semi-custom AQFP design flow


Verilog/VHDL

```verilog
always @([data_in, sh_ctrl, sh_amt])
case(sh_ctrl)
  2'b00 : data_out = data_in <<
  2'b01 : data_out = data_in >>
  2'b10 : data_out = $signed(data
  2'b11 : data_out = $signed(data
  default : data_out = data_in;
endcase
```

Schematic

Digital Sim.

SystemVerilog models, timing models & testbenches

Design rule checks (Assura format)

Physical layout generation

Physical placement on chip

Chip arrival & testing

Chip fabrication

Cadence Virtuoso environment

Open-source software

Developed in this work (or in previous works)

Circuit database, configuration files, models, scripts, etc. developed in this work (or in previous works)

Cell library (OA format)

System simulation, data processing scripts
**MANA microarchitecture**

- **Goal:** Demonstrate AQFP can do both logic and memory
- **RISC-like datapath + dataflow-like control**
- **In-order, single-issue**
- **4-bit data word size**
- **16-bit instr. word**
- **Program branching**
- **21,460 JJs in 1 x 1 cm² chip**
- **30 fJ/op at RT @ 5 GHz**
- **4-phase 5 GHz clock**
- **Latency:** 108 clock phases or 27 cycles (5.4 ns @ 5 GHz)

**MANA – Monolithic Adiabatic iNtegration Architecture**

- Instruction Buffer, Decode, and Issue (IDI)
  - 5,596 JJs
  - 8 cycles (32 phases)

- Register File with external I/O (RFX)
  - 8,142 JJs
  - 8 cycles (32 phases)

- ALU-Shifter (EX)
  - 2,238 JJs
  - 9 cycles (36 phases)

- Ctrl buffer, routing, write-back (WB)
  - 5,484 JJs
  - 17 cycles (68 phases) overlapped 2 cycles (8 phases) write-back

MANA featured in media

Superconducting Microprocessors? Turns Out They’re Ultra-Efficient

The 2.5 GHz prototype uses 80% less energy than its semiconductor counterpart, even accounting for cooling.

By Michelle Thompson

The MANA microprocessor, designed by MANA, Inc., is a superconducting microprocessor that uses quantum computing principles to perform tasks more efficiently than traditional microprocessors.

Manu featured in media

IEEE Spectrum

SUPERCONDUCTOR WEEK

MANA featured in media

SUPERCONDUCTOR WEEK

4 mm

RFX

CTRL BFR + WB

EX

CrAtY

CRAVITY

12
Estimates for an AQFP supercomputer


<table>
<thead>
<tr>
<th>FLOP Type</th>
<th>Single chip TFLOPS</th>
<th>Total PFLOPS in LR280 capacity</th>
<th>GFLOP/J</th>
<th>EFLOPS of 20 MW system</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NVIDIA GA100</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single-precision (AQFP-A)</td>
<td>19.5</td>
<td>1306.15</td>
<td>653.07</td>
<td>13.06</td>
</tr>
<tr>
<td>Double-precision (AQFP-A)</td>
<td>9.7</td>
<td>649.72</td>
<td>324.86</td>
<td>6.50</td>
</tr>
<tr>
<td>Single-precision (AQFP-B)</td>
<td>19.5</td>
<td>326.54</td>
<td>163.27</td>
<td>3.27</td>
</tr>
<tr>
<td>Double-precision (AQFP-B)</td>
<td>9.7</td>
<td>162.43</td>
<td>81.22</td>
<td>1.62</td>
</tr>
<tr>
<td><strong>Intel Polaris</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single-precision (AQFP-A)</td>
<td>1.63</td>
<td>2328.57</td>
<td>1164.29</td>
<td>23.29</td>
</tr>
<tr>
<td>Single-precision (AQFP-B)</td>
<td>1.63</td>
<td>582.14</td>
<td>291.07</td>
<td>5.82</td>
</tr>
</tbody>
</table>

A – assumes 1:1 JJ:transistors; B – assumes 4:1 JJ:transistors
(Physical logistics of fitting all chips into cooling system not considered.)

US Dept. of Energy (DOE) – Exascale Computing Initiative Goal:
1 EFLOPS @ 20 MW

AQFP exceeds DoE requirement even in the conservative cases.

Key challenges for large-scale AQFP

How do we move forward with AQFP logic?

Area efficiency
- Advanced process such as MIT LL SFQ5ee [1]
- Directly coupled QFP (DQFP) [2]
- Novel compact memory
- MAJ5 logic gates

Design methodology
- Multiple phases per row

Latency / clock distribution
- Delay line clocking [3]
- Power divider clocking [4]
- Power-clock distribution via dedicated layers or MCM

Interconnect drivability
- Boosters for long interconnect

Flux trapping
- Moat embedded interconnects [5]

Advanced EDA tools
- Flux trapping analysis [6]
- Flexible chip-level integration tools [7]
- More mature tools [7]

[7] IARPA SuperTools research program
Improving area efficiency

Conventional AQFP buffer with advanced process [1]

- **20 µm × 40 µm**
- **AIST HSTP process**
- **4 Nb layer 100 µA/µm²**
- **dc SQUIDs and transformers are stacked to reduce 70% area**

MIT LL SFQ5ee process

- **15 µm × 20 µm**
- **8 Nb layer 100 µA/µm²**

Directly coupled AQFP [2]

- **20 µm × 25 µm**
- **AIST HSTP process**
- **4 Nb layer 100 µA/µm²**
- **Output transformer removed**
- **Kinetic inductance can be exploited**
- **π-JJs can simplify design**

MAJ5 logic gates

- 5-input majority gates (MAJ5) enables further logic optimization
- Demonstrated MAJ5 in 8-bit KS-adder
- 20% reduction in JJs and latency
- Ongoing challenges:
  - Improve power-clock amplitude margins
  - Improve output current levels

![Image of MAJ5 logic gates](image-url)

![Graph showing signal transitions](graph-url)

- AC1
- S0
- S1
- S2
- S3
- S4
- S5
- S6
- S7
- carry

- 0+FF, 1+FF, one hot, 2+2, FF+FF, random signals
AQFP RAM cell

16x4b RF using AQFP logic gates

Compact AQFP memory cell [1] – requires strong drivers for XY control lines

Improving output driving strength of AQFP

Buffer’s drivable interconnect length: ~0.7mm (FOs, logic gates worse)

Severe design limitation: repeaters increase latency and hardware

Output current boosters developed: single driver, FO2 driver

Improved drivable length to ~2 mm

Enables possibility of more compact AQFP RAM

Signal current is decreasing when inductance of line (length) is increasing.

Two types of booster cells

Revisit AQFP RAM cell
Conventional 4-phase clocking has high latency – 50 ps per logic stage or 4 logic stages/cycle @ 5 GHz

N-phase and delay-line clocking enables low latency operation – 5~10 ps per stage or 20-40 logic stages/cycle @ 5 GHz

Stricter timing constraints for long interconnects

Clocking – skew management

- Long meanders of ac clock lines accumulate significant clock skew at chip-level
  - Limits system clock frequency of large designs
- Scalable microwave H-tree ac clock network constrains accumulated skew to only local blocks [1]
- Best implemented with dedicated Nb-layers for clocking or flip-chip processes

Towards practical applications

- Towards 16-bit general purpose microprocessors [1]
- Quantum computing systems [2]
- Reversible computing systems [3]
- Photon detector systems [4]
- Crypto-accelerators [5] and AI-accelerators

Use hybrid AQFP-SFQ to serially read-out JPO phase.

## Summary

### Area efficiency
- **Cell-level**
  - Advanced process such as MIT LL SFQ5ee [1]
  - Directly coupled QFP (DQFP) [2]
  - Novel compact memory
  - MAJ5 logic gates

### Latency / clock distribution
- Delay line clocking [3]
- Power divider clocking [4]
- Power-clock distribution via dedicated layers or MCM

### Interconnect drivability
- Boosters for long interconnect

### Flux trapping
- Moat embedded interconnects [5]

### Advanced EDA tools
- Flux trapping analysis [6]
- Flexible chip-level integration tools [7]
- More mature tools [7]

### AQFP Logic
- Superconductor logic using Josephson junctions operating adiabatically
- Energy dissipation: 1.4 aJ/op at 5GHz (includes cooling)

### MANA processor
- 4-bit prototype design to show AQFP logic can do both processing and storage
- First demonstration of adiabatic computing using superconductor logic

### AQFP has promise in quantum, reversible, crypto, AI, and sensing applications

### Promising technology platform for next gen data centers and supercomputers – but still several scaling challenges

### Overcoming above challenges will enable large-scale performance-driven designs
Thank You

This work was supported by the Grant-in-Aid for Scientific Research (S) No. 19H05614 and the Grant-in-Aid for Scientific Research (C) No. 21K04191 from the Japan Society for the Promotion of Science (JSPS). This work was also supported by the Office of the Directory of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA) via the US Army Research Office grants W911NF-17-1-0120 and W911NF-17-9-0001.

This work was also supported by the VLSI Design and Education Center (VDEC) of the University of Tokyo in collaboration with Cadence Design Systems, Inc.

The circuits were fabricated in the Clean Room for Analog-digital superconductiVITY (CRAVITY) of the National Institute of Advanced Industrial Science and Technology (AIST) using the high-speed standard process (HSTP). Circuits were also fabricated by MIT Lincoln Laboratory using the SFQ5ee process under the IARPA SuperTools program.