Design Methodologies and Circuits for Superconductive Systems

Professor Eby G. Friedman

Department of Electrical and Computer Engineering
University of Rochester
www.ece.rochester.edu/~friedman

ISCA ’22
DISCoVER Workshop
June 19, 2022
- DISCoVER objectives in circuits and architecture
- Single flux quantum circuits
- VLSI complexity superconductive systems
- Summary
Agenda

- DISCoVER objectives in circuits and architecture
- Single flux quantum circuits
- VLSI complexity superconductive systems
- Summary
This thrust will develop circuits and architectures for VLSI complexity, high performance, ultra-low power superconductive systems

• Develop novel circuits/architectures in support of evolving superconductor technologies
• Develop design techniques and methodologies that support large scale high complexity superconductive systems
• Solve long term issue of superconductor memory
  › Working with our materials team developing novel devices
• Demonstrate several large scale integrated systems
  › SuperSoCC
  › Working with our systems integration and applications team
Agenda

- DISCoVER objectives in circuits and architecture
- Single flux quantum circuits
- VLSI complexity superconductive systems
- Summary
Josephson Junctions (JJs)

- **Two superconductor layers separated by weak link**
  - Insulator, normal metal layer, or constriction

- **Voltage-phase relation**
  - \( U(t) = \frac{\hbar}{2e} \frac{\partial \phi}{\partial t} \)

- **Current-phase relation**
  - \( I(t) = I_c \sin \phi(t) \)

- **\( \phi \) - phase difference across junction**
  - Quantum mechanical parameter

- **Critical current - \( I_c \)**
  - Affected by junction parameters and environment

- **Critical temperature**

- **Critical magnetic field**

- **\( \Phi_0 = \frac{\hbar}{2e} \) - magnetic flux quantum**

Information represented as single flux quantum (SFQ) pulse
- Instead of voltage levels

SFQ pulses exhibit quantized area
- \( \int V(t)dt = \phi_0 = \frac{h}{2e} = 2.07 \text{ mV} \cdot \text{ps} \)

SFQ pulses naturally generated and reproduced
- By overdamped JJs

Modern rapid SFQ (RSFQ) circuits utilize inductors and JJs for interconnect
- DC bias current

Other JJ-based logic families exist
- AC biased: AQFP, RQL
- DC biased: eSFQ, dual rail SFQ

Superconductive Logic for Large Scale Systems

- **High energy efficiency**
  - Two to three orders of magnitude lower energy per operation
  - Including cost of refrigeration

- **SubTerrahertz clock frequencies**
  - Tens to hundreds of gigahertz

![Graph showing power and delay comparison between CMOS and SCE technologies.](image)
Design Gap in SFQ Circuits

- Modern SCE fabrication technologies enable VLSI capability
  - MIT Lincoln Laboratory fabrication
    - SFQ4ee, SFQ5ee, and newer
  - Over $10^6$ Josephson junctions (JJs) per die
- Demonstrated on scalable circuits with regular structure
- Practical circuits exhibit significantly lower complexity
- Need circuits, architectures, and design methodologies targeting SFQ

Agenda

- DISCoVER objectives in circuits and architecture
- Single flux quantum circuits
- VLSI complexity superconductive systems
- Summary
### EDA Flow for SFQ Circuits

- **SFQ circuits require tools analogous to CMOS tools**
  - For all stages of design flow and abstraction levels
  - Reminds me of CMOS in 1985

- **RSFQ circuits however drastically differ from CMOS in many ways**
  - EDA tools require novel guidelines and rules to operate

<table>
<thead>
<tr>
<th></th>
<th>Synthesis</th>
<th>Simulation/Modeling</th>
<th>Verification/Testability</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Register transfer</strong></td>
<td>Automated synthesis</td>
<td>RTL simulation</td>
<td>Functional verification</td>
</tr>
<tr>
<td><strong>Logic gate</strong></td>
<td></td>
<td>Static timing analysis (STA)</td>
<td></td>
</tr>
<tr>
<td><strong>Circuit</strong></td>
<td>Automated layout (place and route) Clock tree synthesis</td>
<td>Dynamic circuit simulation</td>
<td>Layout versus schematic (LVS)</td>
</tr>
<tr>
<td><strong>Layout</strong></td>
<td></td>
<td>Impedance extraction Technology CAD</td>
<td>Design rule check (DRC)</td>
</tr>
<tr>
<td><strong>Device</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Enabling Large Scale Superconductive Computing Systems

- Interconnect
- Bias distribution
- Novel logic families
- Synchronization
- Memory
- SuperSoCC

Device models | Layout | Circuit design | Algorithms | Methodology
--- | --- | --- | --- | ---
Enabling Large Scale Superconductive Computing Systems

Device models

Layout

Circuit design

Algorithms

Methodology

Interconnect

Bias distribution

Novel logic families

Synchronization

Memory

SuperSoCC

DISCOVER Expedition
Two distinct types of interconnect

Active Josephson transmission line (JTL)
- Chain of grounded biased JJs
- Each JJ regenerates degraded signal

Passive transmission line (PTL)
- Superconductive stripline or microstripline
- Impedance matched driver and receiver circuits
- Ballistic propagation of SFQ pulses

SFQ gates have fanout of one
- Require splitter gates to provide multiple output flux quanta
Inductive Noise Coupling in SFQ Circuits

- SFQ circuits highly sensitive to inductive noise coupling
- Many sources of noise exist in multilayer circuits
- Characterizing magnitude and effects of noise in common structures

Flux Trapping in SFQ Systems

- Normal region surrounded by superconductive regions
- Flux trapping can cause asymmetry
  - As cool down below $T_c$
    - Flux trapped in pockets
- Moats
  - Trap excess flux in safe places
- Parallel narrow line with mΩ resistor
  - Thinner linewidth
  - Manage flux trapped in JJs and wide metal lines
- Parallel narrow lines
  - Less area
  - Resistance is frequency dependent

Guidelines for Automated Routing

- Tradeoffs among different types of interconnect
- JTL appropriate for short distances
- PTL suitable for medium and long interconnect

### Repeater Insertion in PTL Interconnect

- **Resonance effects in long PTLs degrade parameter margins**
  - Due to reflections
  - Timing coincides with round trip time of signal

- **Repeaters partition long lines into segments**
  - Compensates for resonance in long PTLs
    - Margins depend on frequency and length

\[ L = \frac{nV_{\text{phase}}}{2f_n} = \frac{n}{2f_n \tau} \]

---


Novel Splitter Circuits

- **Active splitter trees with shared JJs**
- **Passive splitters**
- **Multi-output splitters**
  - Manage area, delay, and bias currents

Enabling Large Scale Superconductive Computing Systems

- **Interconnect**
- **Bias distribution**
- **Novel logic families**
- **Synchronization**
- **Memory**
- **SuperSoCC**

Device models  Layout  Circuit design  Algorithms  Methodology
Synchronization in SFQ Circuits

- Synchronous SFQ circuits operate at high clock frequencies
  - Tens to hundreds of gigahertz
- Most logic gates need to be clocked
- Multiple solutions exist to manage complexity
  - Asynchronous operation
  - Mixed timing approaches

---

QuCTS - single flux Quantum Clock Tree Synthesis

- **Clock skew scheduling**
  - Optimize clock arrival time for sequential logic circuit
  - Exploit useful skew
  - Maximize performance
  - Ensure robustness

- **Clock tree topology**
  - Binary RSFQ splitter tree
  - Minimize wire length
  - Insert JTLs to save wire length

- **Clock network synthesis**
  - First RSFQ clock tree layout tool
  - Placement of delay elements
  - Wire snaking to balance delay
  - Non-negligible splitter area

Optimized clock schedule

<table>
<thead>
<tr>
<th>Instance</th>
<th>Arrival time (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>buffer168</td>
<td>24.226</td>
</tr>
<tr>
<td>buffer611</td>
<td>-35.397</td>
</tr>
<tr>
<td>not193</td>
<td>-2.392</td>
</tr>
<tr>
<td>xor5674</td>
<td>0.487</td>
</tr>
<tr>
<td>xor78</td>
<td>0.891</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

Synthesized clock network layout

Clock Skew Scheduling

- Similar to CMOS clock skew scheduling
  - Although almost every SFQ logic gate needs to be individually synchronized
    - Exacerbates clock distribution design process

---


---

```verilog
module amd2901 ( ck, i, a, b, d, 
    r0_in, r0_out, r3_in, r3_out, 
    q0_in, q0_out, q3_in, q3_out, 
    ovr, zero, signe, np, ng, cin, 
    cout, y );
input ck ;
input [8:0] i ;
...
assign y[1] = rsfq_pb_net4597;
assign y[0] = rsfq_pb_net3835;
...
or_00a ctmi_2089 ( .A ( 
    rsfq_pb_net2763 ), .B ( 
    rsfq_pb_net664 ), .CK ( ck ), 
    .Q ( ctmn_1887 ) );
...
```

---

<table>
<thead>
<tr>
<th>Clock period</th>
<th>44 ps</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Instance</strong></td>
<td><strong>Arrival time (ps)</strong></td>
</tr>
<tr>
<td>inout</td>
<td>0.000</td>
</tr>
<tr>
<td>buffer168</td>
<td>-35.397</td>
</tr>
<tr>
<td>buffer611</td>
<td>-35.397</td>
</tr>
<tr>
<td>not193</td>
<td>-35.397</td>
</tr>
<tr>
<td>xor567</td>
<td>0.487</td>
</tr>
<tr>
<td>xor78</td>
<td>2.435</td>
</tr>
<tr>
<td>and152</td>
<td>3.426</td>
</tr>
<tr>
<td>or547</td>
<td>10.424</td>
</tr>
</tbody>
</table>

...
Clock Tree Synthesis

- **CTS algorithm for SFQ circuits**
- **Tested on AMD2901 layout**
  - 1,050 gates
  - 1,049 splitters
  - Runtime – 9 hours
- **Max delay imbalance**
  - 1.6 ps

---

Enabling Large Scale Superconductive Computing Systems

Device models  Layout  Circuit design  Algorithms  Methodology
Bias Distribution in SFQ Circuits

- Each gate requires appropriate bias current
  - Supplied by multiple input pads

- Objectives of bias distribution network
  - Improve robustness (margins)
  - Decrease power dissipation
  - Smaller bias structures

- Need energy efficient SFQ circuit design guidelines
Resistive Bias Distribution (RSFQ)

- **Bias current distributed by resistive network**
  - Dissipates significant static power through Joule heating

- **Size of resistor can be decreased**
  - Decreases static power dissipation
  - Increases redistribution of bias current between different gates
    - Data dependent
    - Lowers clock frequency

---

- Replace resistors with inductors
  - Superconducting inductors distribute bias current
- Josephson junctions behave as current regulators (limiters)
- Voltage bias bus has highest switching frequency
- JJs in clock distribution network switch every cycle
  - Clock JTLs have maximum average gate voltage
- Feeding JTL connected to clock network
  - Source of maximum average voltage
  - $V = \Phi_0 f_{\text{clk}}$
Multiple new components introduced in ERSFQ
- Bias JJs, bias inductors, feeding JTL, parasitic components
- Require guidelines for automated synthesis

FJTL requires significant area
- 10% to 50% of circuit area

Hypres
- **RSFQ gates typically biased in parallel**

- **Serial biasing (current recycling) drastically reduces bias current**
  - Voltage stacking in CMOS
  - To date only used in highly regular circuits
    - Shift registers

- **Partition arbitrary circuit into segments**
  - Graph partitioning problem
  - Additional constraints
    - Same bias current
    - Small differences in bias can be tolerated
  - Proposed partitioning during placement
  - Dummy structures equalize bias currents
RSFQ gates typically biased in parallel

Serial biasing (current recycling) drastically reduces total bias current

Partitioning arbitrary circuit into segments
- During placement process
- Graph partitioning problem
- Dummy structures equalize bias currents

~ 15 to 20% of cut nets
~ 1% bias imbalance

Pull gates into corners
- Four partitions

Enabling Large Scale Superconductive Computing Systems

Interconnect

Bias distribution

Novel logic families

Synchronization

Memory

SuperSoCC

Device models
Layout
Circuit design
Algorithms
Methodology
Memory in Superconductive Circuits

- **Superconductivity provides advantages for memory**
  - Persistent storage of magnetic flux
  - No refresh necessary

- **Memory density – major issue**
  - Magnetic flux quanta stored in inductors
  - Inductor size difficult to scale
  - CMOS DRAM based on capacitors
Memory Technologies for SFQ Circuits

- **Superconductive SFQ-based cells**
  - Persistent storage of magnetic flux
  - No refresh necessary
  - Magnetic flux quanta stored in inductors
    - Difficult to scale
  - Higher density cells not drivable by SFQ pulses

- **Cryogenic CMOS DRAM**
  - High density
  - Requires separate ICs and related interfaces

- **Spin-based memory**
  - Can be integrated on same IC
  - Scalable to high densities
  - Can be driven by SFQ pulses
Spin-Based Cryogenic Memory Cell

- Nanocryotron (nTron) used as driver
  - Novel nanowire electrothermal device
- Gate current creates resistive hotspot
- Disrupts superconductivity in channel
- Diverts bias current into load
  - Spin-based element
- Can be triggered by SFQ pulse

Superconductor Ferromagnetic Transistor (SFT)

- Three and four terminal devices
  - Provides functional switch
- Stack of superconductor, ferromagnetic, and insulator layers
- Injector current changes superconductive energy gap in acceptor
  - Changes critical current of acceptor JJ

**Compact model of superconductor ferromagnetic transistor**

- Three terminal device composed of superconductor (S), ferromagnetic (F), and insulator (I) layers

\[ I_i(l_i) \cdot \sin \phi \]

\[ I_i + I_a \]

G. Krylov and E. G. Friedman, “Compact Model of Superconductive-Ferromagnetic Transistor,” *Proceedings of the IEEE Symposium on Circuits and Systems*, May 2018
Enabling Large Scale Superconductive Computing Systems

- Interconnect
- Bias distribution
- Novel logic families
- Synchronization
- Memory
- SuperSoCC

Device models | Layout | Circuit design | Algorithms | Methodology
State Storage Loops in RSFQ

- Composition of SFQ gates
  - Storage loops
  - Decision making pairs

- Most RSFQ gates require clock signal to operate
  - Signaling convention
  - Persistent storage of state

- Incoming clock pulse switches specific JJs
  - Resets stored state
  - Produces output based on state
    - Presence or absence of SFQ pulse

- Without clock need method to reset storage loop (state)
Self-Resetting Storage Loops => DSFQ

- **Resistive elements introduced into storage loops to dissipate flux**
  - Extend retention time

- **Dynamic SFQ (DSFQ)**
  - Based on novel design from IBM
  - Longer, gradual leakage time
  - Faster reset

---

- Resistive elements introduced into RSFQ storage loops to dissipate flux
  - Asynchronous operation
- Majority gates
  - Three, five, and more inputs
  - Multiple benefits for logic synthesis
    › Enhance logic complexity
    › Reduced logic depth
    › Higher throughput

All-Josephson Junction Inductor-less Circuits

- Based on bistable Josephson junctions
  - Existence of second harmonic in sinusoidal current-phase relationship
    \[ I = A \sin(\phi) \pm B \sin(2\phi) \]
- Verilog-A model
- All-JJ logic cells
  - Lower area, delay, and bias current
  - No longer need inductive loops
- Supports scaling of SFQ structures to nanometer feature sizes

Storage Element with Different JJs

Conventional 0-JJs

Stacked 0-JJs

π-JJ

π-JJ and 0-JJs

Fewer stacked JJs

Bistable JJs

0-π JJ or 2φ-JJ

- **RSJC model of JJ**
  - \[ I = A \sin(\phi) + B \sin(2\phi) + \alpha \dot{\phi} + \ddot{\phi} \]

- **Verilog-A model**
  - Critical current density, \( J_c \)
    - 0.4 to 0.6 kA/cm\(^2\)
  - Capacitance
    - \( C = 4.5 \times 10^{-6} \) fF/\( \mu \)m\(^2\)
  - \( R_{shunt} \) included in damping coefficient of JJ
## Comparison Between All-JJ and 0-JJ Complex Cells

<table>
<thead>
<tr>
<th></th>
<th>c17 circuit with 0-JJ</th>
<th>c17 circuit with 2φ-JJ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Critical current density</td>
<td>1 kA/cm²</td>
<td>0.5 kA/cm²</td>
</tr>
<tr>
<td>Delay</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• AND</td>
<td>~ 22 ps</td>
<td>~ 8 ps</td>
</tr>
<tr>
<td>• NOT</td>
<td>~ 20 ps</td>
<td>~ 7 ps</td>
</tr>
<tr>
<td>Bias current*</td>
<td>~ 22 mA</td>
<td>~ 13 mA</td>
</tr>
<tr>
<td>Inductance length</td>
<td>~ 0.8 to 1 mm</td>
<td>-</td>
</tr>
<tr>
<td>Storage loop</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* One stage JTL included at input and output of each cell
Enabling Large Scale Superconductive Computing Systems

- Interconnect
- Bias distribution
- Novel logic families
- Synchronization
- Memory
- SuperSoCC

Device models | Layout | Circuit design | Algorithms | Methodology
- System demonstration testbed comprising heterogenous computing fabric
  - Operating across multiple temperature zones

- Three stage cryogenic interface

- SuperSOCC – I
  - Exploits existing SFQ technology

- SuperSOCC – II
  - Exploits novel design methodologies and all-JJ logic
Agenda

- DISCoVER objectives in circuits and architecture
- Single flux quantum circuits
- VLSI complexity superconductive systems
- Summary
Summary

- Data centers and cloud computing continue to increase in demand
  - Growing energy requirements for stationary systems
- **SFQ is highly energy efficient, high speed technology**
  - Orders of magnitude lower energy and higher speed than CMOS
  - Natural technology for stationary systems such as cloud computing
  - All-JJ inductor-less technology enables deep scaling
- **SFQ-specific design methodologies and automation required to achieve VLSI complexity superconductive systems**
  - Multiple circuit and design methodologies in development
  - Multiple EDA/algorithmic efforts in development
- **Additional important applications**
  - Space-based electronics
  - Quantum computing
Shameless Plug for Recent Book on SFQ Circuit Design

- Appeared this past fall 2021
- Springer Publishers
  - Chuck Glaser, Editor
Cryocooling for Superconductive Electronics

### Most power efficient, current supercomputers
- 10 to 20 GFLOP/J

### Currently #1 in Top500 supercomputers
- Fugaku (Japan) – as of 11/2020
  - 30 to 40 MW (total)
  - 442 PFLOP/s
  - 16.87 GFLOP/W

---

- RSFQ circuits drastically differ from CMOS in many ways
- EDA tools require novel guidelines and rules to operate
**Overbiased and Underbiased ERSFQ Circuits**

- **Insufficient current (underbiased condition)**
  - Supply less than target bias current (e.g., 85%)
  - Load bias decreases

- **Excess current (overbiased condition)**
  - Supply more than target bias current (e.g., 115%)
  - Load bias increases
  - Power dissipation increases

\[ I_B = 0.7 \, I_C \]
\[ I_B = 1.3 \, I_C \]

G. Krylov and E. G. Friedman, “Design Methodology for Distributed Large Scale ERSFQ Bias Networks,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 11, pp. 2438–2447, November 2020
Source of Inductance in All-JJ Circuits

- **Long interconnect between JJs**
  - Linear inductance
  - Small inductance

- **Parasitic inductance**
  - Vias
  - Short interconnect between JJs

Effects of Inductance on All-JJ Circuits

- Control current distributions
- Prevent reflected pulses at input
- Improve margins
  - Dependency of cell operation on JJs
    - Small parameter variations
- Small increase in delay
Coupling Noise in All-JJ Circuits

- **Parasitic inductance**
  - Vias
  - Short distance between JJs
  - Dominant parameters

- **Disturbs current distribution**

- **Degrades cell operation**

- **Decreases margins**
- Wide data bus carries clock signal for data
- Exploits ambiguous representation of data and clock
  - Reduces area of wide data buses
- Can be used for shared interconnect
  - Widely used in CMOS SOC
**Meissner Effect**

- **Magnetic field does not penetrate superconductor**
  - Perfect conductivity is not reason

- **Magnetic field inside “perfect conductor” at $T < T_c$**
  - Depends on magnetic field during cooling
  - Field introduced when $T > T_c$ remains
  - Field introduced when $T < T_c$ expelled

- **Magnetic field inside superconductor**
  - Always expelled when $T < T_c$

- **Persistent screening surface currents**
  - Cancel external field
  - Critical field $\leftrightarrow$ critical current density

---

Applications of DSFQ Majority Gates

- Multiple benefits for logic synthesis
  - Can optimize complex logic
  - Can reduce logic depth
- Increase throughput

---

- **Computers began to specialize after 1960’s**
  - Classified by total power consumption

- **Recent trends**
  - Increased demand for low power applications
  - Increased demand for fast, large scale computers
    › Supercomputers, data centers

![Diagram showing the evolution of computing systems over time with power consumption on the y-axis and time from 1950 to 2010 on the x-axis.](image)
Asynchronous RSFQ Circuits

- Clock and data signals represented equally in RSFQ
- C elements require small area
- Any non-inverting RSFQ logic gate can be self-timed
  - Apply data pulses to clock input
  - Requires splitters and mergers
    - Additional area and delay
  - Additional timing constraints
    - Sensitive to input skew
  - Possible race condition
    - Clock path should be slower than data path

- **Energy efficient SFQ circuit design guidelines**
  - Automated evaluation of design parameters
- **Layout techniques to minimize inductive coupling to sensitive SFQ gates**

G. Krylov and E. G. Friedman, “Design Methodology for Distributed Large Scale ERSFQ Bias Networks,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 11, pp. 2438–2447, November 2020
Guidelines for bias and parasitic inductances

Bias inductance behavior matches analytic expression

Feeding JTL Size

- Tradeoffs based on FJTL size
- FJTL size dependence
  - Variations of supplied bias current
  - Target bias margins of system

G. Krylov and E. G. Friedman, “Design Methodology for Distributed Large Scale ERSFQ Bias Networks,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 11, pp. 2438–2447, November 2020
Sense Amplifier Topology

- Synchronous DC-SFQ converter used as sense amplifier
- Exploits shape of nTron output waveform
- Applicable to devices with low magnetoresistance
- High clock frequency increases accuracy

Behavior of SFT Model

- DC behavior as compared to experimental data
  - 7.4% mean absolute error

- Transient operation matches expected behavior

- Memory for cryogenic computing
- Integration of various devices and technologies
- Memory array development
- Readout circuits for cryogenic memory cells

IARPA SuperTools Program

- **Current state-of-the-art superconductive circuits**
  - 800,000 Josephson junctions in serialized pattern (shift register)
  - 11,000 Josephson junctions in complex circuit (microprocessor)

- **EDA tools for superconductive electronics**
  - Currently no large scale CAD tools
  - No established cell libraries
  - Circuits and layouts designed on *ad hoc* basis

- **Program to develop EDA tools and methodologies**
  - Cell libraries
  - Place and route
  - Power delivery network/current biasing
  - Clock tree synthesis
Current EDA Tasks for Superconductive Electronics

- **Power delivery for SFQ circuits**
  - Inductive coupling/flux trapping
  - Bias networks

- **Clock tree synthesis for SFQ**
  - H-tree synthesis
  - Clock skew scheduling
  - Clock network synthesis

- **Current recycling**
  - Circuit partitioning

- **Advanced circuit/interconnect topologies**
  - Repeater insertion
  - Dynamic SFQ
  - Novel splitters

- **Thermal behavior of Josephson junctions**
Global Signaling for RSFQ Circuits

- **Energy of SFQ interconnect**
  - Josephson transmission lines (JTL)
    - $10 \times 10^{-19} J$ per stage
  - Passive transmission lines (PTL)
    - $6 \times 10^{-19} J$ per stage

- **Repeater insertion for SFQ logic**
  - Resonance frequency @ 20 GHz: 2.9 mm
  - Resonance frequency @ 40 GHz: 1.35 mm

- **Energy of SFQ interconnect**
  - Josephson transmission lines (JTL)
    - $10 \times 10^{-19} J$ per stage
  - Passive transmission lines (PTL)
    - $6 \times 10^{-19} J$ per stage

- **Repeater insertion for SFQ logic**
  - Resonance frequency @ 20 GHz: 2.9 mm
  - Resonance frequency @ 40 GHz: 1.35 mm

Self-heating due to switching JJ into resistive state
- Bottom electrode of niobium JJ
- Temperature affects switching properties
Integrate multiple devices into simulation environment

- Nanocryotron (nTron)
- Josephson junction (JJ)
- STT-MRAM
- Spin valve (SV)

JJ to nTron to STT-MRAM

JJ driving nTron switching MTJ
- **Common method for semi-custom design of large scale circuits**

- **Standard cells**
  - Separately designed and optimized
  - Characterized standalone and with other gates
  - Exhibit known delays and variations
    - Stored in look-up tables
  - Arranged into cell rows and placed by an automated tool

- **Routing channels**
  - Space between rows reserved for signal routing
- **Novel globally asynchronous, locally synchronous (GALS) clock activation technique**
- **Shared circular interconnect for large scale SFQ systems**

Proposed and characterized novel majority gates
- Three, five, and more inputs

Delay and area comparable to AND gate
- Larger due to additional input

Partitioning with Move Based Algorithm

- **Partitioning of netlist during placement**
  - Computationally complex
  - Intrusive for placement process
  - Better results
    - ~ 15-20% of cut nets
    - ~ 1% bias imbalance


<table>
<thead>
<tr>
<th>Benchmark circuit</th>
<th>Bias current, mA</th>
<th>Vertices (gates)</th>
<th>Edges (nets)</th>
<th>Two partitions</th>
<th>Four partitions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cuts</td>
<td>Bias imbalance</td>
<td>Bias difference, mA</td>
<td>Maximum bias current, mA</td>
<td>Cuts (total)</td>
</tr>
<tr>
<td>s27</td>
<td>8</td>
<td>4.8%</td>
<td>0.6</td>
<td>13.7</td>
<td>15</td>
</tr>
<tr>
<td>s298</td>
<td>70</td>
<td>1.3%</td>
<td>2.5</td>
<td>192</td>
<td>125</td>
</tr>
<tr>
<td>s344</td>
<td>75</td>
<td>1.5%</td>
<td>2.8</td>
<td>191</td>
<td>125</td>
</tr>
<tr>
<td>s420</td>
<td>96</td>
<td>1.1%</td>
<td>2.9</td>
<td>278</td>
<td>180</td>
</tr>
<tr>
<td>s1238</td>
<td>390</td>
<td>0.02%</td>
<td>0.2</td>
<td>758</td>
<td>657</td>
</tr>
<tr>
<td>amd2901s</td>
<td>459</td>
<td>0.01%</td>
<td>0.3</td>
<td>1,109</td>
<td>650</td>
</tr>
<tr>
<td>amd2901f</td>
<td>205</td>
<td>1.8%</td>
<td>30</td>
<td>1,671</td>
<td>669</td>
</tr>
</tbody>
</table>
Geometric Partitioning with Simulated Annealing

- Partition based on coarse placement
- Optimize partition boundaries
  - Simulated annealing used as example
- Worse partition characteristics but less intrusive
  - Possible improvement with better coarse placement

---

**TABLE II: Results of geometric partitioning on modified ISCAS'89 benchmark circuits and the AMD2901.**

<table>
<thead>
<tr>
<th>Benchmark circuit</th>
<th>Two partitions</th>
<th>Two partitions with optimization</th>
<th>Four partitions with optimization</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cuts</td>
<td>Bias imbalance</td>
<td>Cuts</td>
</tr>
<tr>
<td>s27</td>
<td>6</td>
<td>158%</td>
<td>16</td>
</tr>
<tr>
<td>s298</td>
<td>27</td>
<td>1,198%</td>
<td>104</td>
</tr>
<tr>
<td>s344</td>
<td>90</td>
<td>11%</td>
<td>90</td>
</tr>
<tr>
<td>s420</td>
<td>48</td>
<td>786%</td>
<td>117</td>
</tr>
<tr>
<td>s1238</td>
<td>194</td>
<td>739%</td>
<td>386</td>
</tr>
<tr>
<td>amd2901s</td>
<td>177</td>
<td>109%</td>
<td>318</td>
</tr>
<tr>
<td>amd2901f</td>
<td>77</td>
<td>2,365%</td>
<td>273</td>
</tr>
</tbody>
</table>

---

Compact model for three terminal SFT developed
- Based on RCSJ model of JJ

Injector exhibits resistive properties

Acceptor critical current depends upon injector voltage

Developed in Verilog-A

- **DFT for large scale superconducting circuits**
  - Test point insertion using confluence buffers (CB)
  - Set/scan chains

Synchronization in SFQ Circuits

Isochronous (global clock) → Single phase → H-tree

Isodromous (local clock)

GALS

Elastic pipeline → Concurrent flow
Counterflow
Clock-after-data

Inelastic pipeline

HL-tree

Concurrent flow

Wave pipelined FIFO buffered HCLC

Asynchronous (no clock) → Dual-rail

Data driven self timed (DDST)
RSFQ-AT
Boolean SFQ
Delay insensitive (DI)

Design for Testability for SFQ Systems

- Need to verify functionality of large scale SFQ circuits after fabrication
  - Cryogenic functions and blocks difficult to access
  - Large size prevents *ad hoc* testing

- Design for testability (DFT) widely used in CMOS circuits
  - Enables fast testing of fabricated ICs
  - Enables access to internal functions
- D flip flop used as blocking gate
  - Similar to multiplexer
  - Lower overhead

- Test points inserted into data paths
  - Supply test inputs and extract output data

---

G. Krylov and E. G. Friedman, "Design for Testability of SFQ Circuits," *IEEE Transactions on Applied Superconductivity*, vol. 27, no. 8, pp. 1-7, December 2017
Set/Scan Chains

- Bypass combinatorial logic
- Load test data into specific register
- Extract output of specific logic stage

- Used in CMOS
- Proposed for RSFQ
  - Using blocking gates to reduce overhead
    - As compared to multiplexers

G. Krylov and E. G. Friedman, "Design for Testability of SFQ Circuits," *IEEE Transactions on Applied Superconductivity*, vol. 27, no. 8, pp. 1-7, December 2017
Hardware Security in SFQ Systems

- **Primary application – large data centers for industry and government**
  - Highly sensitive data
  - Hardware security techniques necessary to thwart reverse engineering
Gate Camouflaging

- Camouflaged cells indistinguishable for attacker
  - Perform different (unknown) functions
- Camouflaging approach for SFQ circuits
  - Dummy Josephson junctions
  - Operate as resistor

Logic Locking

- Logic locking adds secret key to unlock circuits
  - Incorrect key produces incorrect/random operation
  - Typically uses multiplexers
    - Costly in SFQ

- Logic locking for SFQ circuits
  - Bias current used as secret key
  - Inductively coupled to gates
  - Incorrect operation without correct key current