Interconnects & Devices for Superconductive Systems

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DISCoVER Expedition Workshop
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Outline

• Intro Comments & Overview
• Interconnects for Cryogenic Electronics
• New Device Technologies
• Concluding Comments
Intro Comments

- **AMNSTC** – A state-funded Micro/Nano Fab & Tech Center @ Auburn University
- **Hamilton Lab** @ Auburn University, Auburn, AL (shown below) http://fast.auburn.edu/
  - Work of multiple students (George Hernandez (@ Intel), Rujun Bai (@ Lam), Simin Zou (@ Applied Materials), Uday Goteti (@ UCSD), Vaibhav Gupta (@ Intel), Bhargav Yelamanchili, Sherman Peek, Archit Shah, Stephen Bankson, as well as others)
- Much of the work shown here (for superconducting flex cables and connectors) was sponsored by Microsoft, working closely with Dr. David Tuckerman
Motivation → Interconnect #’s and $\dot{Q}$

D-Wave processor in a dilution refrigerator (shields removed)

Janis dilution refrigerator with many cables

Janos gmon transmon from UCSB (Martinis)

SCUBA-2 Module for the James Clerk Maxwell Telescope


http://www.janis.com/UHVCompatibleDilutionRefrigeratorForSTM_NanoTechWeb.aspx#
IBM / Google / Intel (among others!)

IBM Hummingbird


Intel Tangle Lake & Horse Ridge II

Intel

Google Bristlecone & Sycamore
IBM / Google / Intel (among others!)

Quite complex and heavily-integrated cryogenic systems realized for cryogenic/microwave quantum computing

A significant amount of recent work to build-up related technologies

Substantial body of work to draw from for DISCoVER Expedition System
Representative SuperSoCC System Diagram

(a) S-MCM
(b) Edge contacts (power)
(c) Core SCE chips (w/ Devices)
(d) SC flex cables (Interconnects)
(e) Interface @ 4 K
(f) Interface @ S-MCM
(g) Area array contacts (signal)
(h) Thermalization approach
Outline

• Intro Comments & Overview

• Interconnects for Cryogenic Electronics
  • Superconducting flexible cables
  • Connectors / connection approaches
  • S-MCM

• New Device Technologies

• Concluding Comments
Previous SC Flex Cable Work

- In previous work, where possible, we’ve used superconductors (SC):
  - Ultra-low (but not zero) loss below $T_c$ @ microwave frequencies
  - (Surrounding) dielectric loss ($\tan\delta$) important, comparable to SC loss
  - Small cross-sections to limit thermal transport
  - Impedance matching similar to non-SC, but sometimes need to take SC kinetic inductance ($L_k$) into account
  - EM simulators (i.e., ADS, HFSS, Sonnet, etc.) with proper SC model

- Example (potential) trace density of SC cables*:
  - Single layer of single-ended stripline: 5 $\mu$m thick PI, ~ 5 $\mu$m wide traces, 5 $\mu$m vias, 20 $\mu$m space between traces and vias...pitch ~ 50 $\mu$m => 200 single-ended / cm (of width) [< 10 nW for 4K-10mK ... 50 pW / trace]
  - Need sufficient grounding between signals to reduce crosstalk and allow impedance matching up to very high frequencies (> 100 GHz, in some cases)
  - Challenge to fan-out/break-out to (available) connectors
  - Incorporate filters and/or attenuators
  - Working to scale to this level, expand to multi-layer, 2D break-out, etc.

* Not what will be shown today, just for motivating the topic
Various Flex Cables Constructed @ AU

<table>
<thead>
<tr>
<th>Name</th>
<th>Length</th>
<th>Material type</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stripline</td>
<td>1 m</td>
<td>Spin-on polyimide</td>
<td>20 μm</td>
</tr>
<tr>
<td>Stripline</td>
<td>5 cm</td>
<td>Spin-on polyimide</td>
<td>20 μm</td>
</tr>
<tr>
<td>Microstrip</td>
<td>1 m</td>
<td>Spin-on polyimide</td>
<td>10 μm</td>
</tr>
<tr>
<td>Microstrip</td>
<td>5 cm</td>
<td>Spin-on polyimide</td>
<td>20 μm</td>
</tr>
<tr>
<td>Embedded Microstrip</td>
<td>5 cm</td>
<td>Spin-on polyimide</td>
<td>25 μm</td>
</tr>
<tr>
<td>Microstrip</td>
<td>1 m</td>
<td>Kapton film</td>
<td>50 μm</td>
</tr>
<tr>
<td>Microstrip</td>
<td>5 cm</td>
<td>Kapton film</td>
<td>50 μm</td>
</tr>
</tbody>
</table>

- Family of flex cables fabricated on different flexible substrates.
- Superconducting microstrip, embedded microstrip and stripline versions.
- Significant amount of process development was/is involved…more to do…
- Latest 5 cm long structures (resonators and transmission lines) have excellent yield.
Microwave Stripline Transmission Line & Resonator Fabrication Process

- HD4100(10um) cured @ 375°C on Cr/Al deposited wafers
- Al/Nb/Al (bottom ground) patterned and deposited on the cured HD4100
- Ti/Cu seed layer patterned and deposited on bottom ground
- Electroplating on the patterned and cured bottom HD4110(20um) @225°C
- Al/Nb/Al (Signal) patterned and deposited on the cured HD4110
- Ti/Cu seed layer patterned and deposited on top of Signal layer
- Electroplating on the patterned and cured top HD4110(20um) @225°C
- Al/Nb/Al (top ground) patterned and deposited on the cured HD4110
- Top protective polyimide HD4100 (4um) patterned and cured @225°C
- Ti/Au UBM layer patterned and deposited on the cured top protective polyimide
- Release from handle
Comparison of Multiple Stripline Samples

- Comparison of insertion loss of multiple stripline samples (normalized to loss per unit length).
- Length normalized insertion loss was well less than 0.1 dB/cm for all samples.
- Stripline length was 25 cm (with 100 µm wide anti-pad under connector pin).
- “Wiggles” / oscillations in $S_{21}$ due to impedance mis-match...actual loss follows the peaks (top envelope, ~ green dashed line in plot) of $S_{21}$

Edge Launch Connector → Indium Bumping (+ Underflow)

- “Chip”-on-flex bonding for both commercial and custom interconnects
  - SAC-to-indium and indium-to-indium

Custom and commercial “chip-on-flex” attachment of 375 °C cured polyimide cables (top) and 225 °C cured polyimide cables (bottom).

Microscopic image of a flex tape Indium bump array bonded to a Si chip with an Indium bump array.

Cable-to-Cable Connection – Face-to-Face

- DC test of R vs. T
- Representative line with a $T_c$ of $\sim 9.0$ K
- All lines in the assembly gave a critical current $I_c$ of $\sim 10$ to $11$ mA
- Survives thermal cycles

- TDR response of 12 SC striplines @ 4K
- Results show very small dip in impedance at the connector region (note this was designed for $Z_0 = 20 \, \Omega$)
- Simulation of pulse transmission using time-domain response

B. Yelamanchili et al., EUCAS (2021).
Signal Integrity Sims in Keysight ADS

“Eye” Diagrams of Guassian Pulses to Represent Single Flux Quanta (SFQ)

New S-MCM Technologies

- Use of Mo as substrate in “MCM”
  - DC test structure shown here, with Nb-based traces (Tc ~ 8.3 K), polyimide dielectric, & In bumps + epoxy underfill

- Advantages include:
  - Less limited substrate size, more rigid, less brittle, shielding

Mo wafer after cleaning

After signal deposition + In plating

Si chip with 20 mm x 20 mm In bump array size after bonding

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• Interconnects for Cryogenic Electronics
• **New Device Technologies**
  • CPR-engineered JJs – candidates for logic circuitry and memory
  • Nanowire devices – candidates for interface electronics
  • New materials & structures to help realize these devices
• Concluding Comments
Integration Challenges

- Large inductances
- Large bias currents
- JJs with phase-shifted current-phase relationships (CPRs), which include devices with intrinsic bistability, and phase-controlled logic circuits reduce the need for large integrated inductors in superconductive digital circuit blocks
  - In this approach, the encoding of digital information departs from using (only) single flux quanta and relies on bistable magnetic JJs in which information is represented by the Josephson energy.
  - The need for physically large (not-scalable) inductors is eliminated, allowing significantly-enhanced scalability.
- We will investigate JJs with engineered CPRs and use them to develop new device technologies for enhanced scaling of superconductive electronics.

Current-Phase Relation (CPR) of JJ

Various types of CPR
- **a** – standard sinusoidal CPR \( I = I_c \sin \varphi \)
- **b, c** – deviation from standard CPR, when \( I_c \) achieved at \( \phi_{\text{max}} \leq \frac{\pi}{2} \) and \( \phi_{\text{max}} \geq \frac{\pi}{2} \)
- **d** – \( \pi \) junction
- **e** – CPR whose energy-phase relation has two minima at \( \phi = 0 \) and \( \phi = \pi \)
- **f** – multivalued CPR that does not correspond to a true Josephson effect and may have various causes


Clear transition to 2nd harmonic

Nb-CuNi-Nb
Schematic view of a complete memory cell consisting of vertically integrated Superconductor-Insulator-Superconductor (SIS’) and magnetic tunnel junction (MTJ). Pictures show magnetic lines of force for:
(a) anti-parallel (AP) magnetization alignment;
(b) parallel (P) magnetization alignment (causes suppression of $I_c$).

The two magnetic states of the MTJ represent binary logic “0” and “1” levels which can be detected using a SIS’ junction.

Superconductive Nanowire Devices

- **nanoCryoTrons (nTrons)**

- **Quantum Phase Slip Junctions (QPSJs)**

Epitaxial NbN and GaN/NbN

- Single-crystalline NbN thin films for superconducting nanowire single-photon detectors (SNSPDs) grown by molecular beam epitaxy (MBE) at high temperature on nearly lattice-matched AlN-on-sapphire substrates.

- Molecular beam epitaxial to growth of AlGaN/GaN quantum-well heterostructure directly on top of an ultrathin crystalline NbN to integrate NbN-based superconductors with the wide-bandgap family of semiconductors.


• Interconnects for superconductive systems:
  • DISCoVER requires high performance interconnection across multiple interfaces (electrical, thermal, mechanical)
  • Leverage previous work on superconducting flexible cables and connectors with demonstrated high performance
  • New interconnect and S-MCM technologies are being created to improve system integration, robustness, and reliability

• Device (and material!) technologies for superconductive systems:
  • Current device technologies are insufficient for the large scale, densely integrated superconductive electronics systems we are aiming for in DISCoVER
  • Research to explore new materials & device technologies is ongoing
  • Realizing new types of junctions (multiple types of JJs and nanowire devices) will help expand the options for device technologies to improve system integration density and capability