High Density Memory Based on Stacked Magnetic and Josephson Junctions

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CryoRAM Requirements

- Can form dense, addressable RAM array (small pitch = memory cell size + safe distance to the next cell)
- Small addressable memory cell (not just small memory element)
- Includes read/sense elements
- Includes write/erase elements
- Energy-efficient
- Does not burn energy in non-selected cells
- Energy is spent only in the selected cell for readout or write operations.
- Reasonable power requirements (i.e. current amplitude) for RAM line drivers
- Fast Read (in ps). Moderately fast Write (< 100 ps)
- Manageable Half-select (i.e. can work with individual cell or raw without affecting neighboring cells)
- Compatible to single flux quantum digital circuits in fabrication, signal and speed levels.
Memory Status to Date

• Most of the work on cryomemory went into the development of new devices (physics and materials) with memory properties, i.e. switchable bistable devices.

• Relatively little effort was in the development of the addressable memory arrays random access memory (RAM), i.e. addressable arrays with fast and energy-efficient read and write.

• Result: despite many years and many millions of dollars:
  - Still no cryoRAM was developed with parameters required for applications or even competitive to the existing all-Josephson junction memory
  - Majority of the developed memory elements were not applicable to make a good RAM

• JJ-memory density is still several orders of magnitude lower than that in memories compatible with the CMOS processes (DRAM, MRAM, SRAM, NOR Flash). In memory applications, usually, the density is more important than the speed.
Josephson memories

1987 NEC Japan,
1024 bit NDRO Josephson memory

1999 NEC Japan, Nagasawa
4096 bit vortex transitional memory
256 x 16 bit organized
tested at 620 MHz
*S. Nagasawa et al., IEEE TAS, Vol. 9, No. 2, p. 3708, 1999

2000 ISTEC SRL Japan, Nagasawa
256 bit vortex transitional memory
all dc-powered

• S. Nagasawa developed a Vortex transition (VT) memory cell – a SQUID based cell
• VT cell was further scaled down using MIT-LL process by V. Semenov (2019) to ~100 μm²
Hybrid CMOS-Josephson memory at UC Berkeley

<table>
<thead>
<tr>
<th><strong>64 kbit (4096 x 16)</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>power consumption</td>
</tr>
<tr>
<td>12 mW read,</td>
</tr>
<tr>
<td>21 mW write</td>
</tr>
<tr>
<td>Read access</td>
</tr>
<tr>
<td>400 ps (experiment)</td>
</tr>
<tr>
<td>Cycle time</td>
</tr>
<tr>
<td>1 ns (1GHz)*</td>
</tr>
<tr>
<td>JJ carrier</td>
</tr>
<tr>
<td>4.5 kA/cm² Hypres,</td>
</tr>
<tr>
<td>5 x 5 mm²</td>
</tr>
<tr>
<td>CMOS</td>
</tr>
<tr>
<td>65 nm TSMC CMOS</td>
</tr>
<tr>
<td>low $V_t$, 2 x 1.5 mm²</td>
</tr>
<tr>
<td>I/O</td>
</tr>
<tr>
<td>5 mV (latching gates)</td>
</tr>
</tbody>
</table>

This is the largest functional 4 Kelvin memory [1].

Cryogenic Magnetic Memory

Hybrid circuits with cryogenic magnetoresistive memory elements (JJ+metal spintronics)

- Memory cell based on spintronic elements with addition of JJs (for low impedance) or nanowire switches (for high impedance)
- Polarized spin injection for magnetization reversal (spin torque transfer)
- JJ periphery (address decoders, sense, etc.)

Superconducting-Ferromagnetic (SF) Junctions (superconducting spintronics)

- Memory cell based on Magnetic JJs (MJJ) w/ or w/o additional JJs or SF switches
- Magnetic field for magnetization reversal (field programmable)
- JJ periphery (address decoders, sense, etc.)
Competition

• Success of room-temperature semiconductor memories are based on the availability of tri-terminal devices (transistors) integrated in the memory cells. Transistors enable cell addressability (cell selection).

• In JJ technology this function can be done using a SQUIDs or nTrons, but they are large circuits.

• Best JJ memories to date:
  • Stony Brook Univ./MIT Lincoln Lab [V. Semenov et al., IEEE Trans. Appl. Supercond. 29, 1302809 (2019)] is based on the Vortex Transitional (VT) memory cell with the SQUID-based cell selector. The cell area is \( \sim 100 \, \mu m^2 \) corresponding to over \( 0.9 \, \text{Mbit/cm}^2 \) functional density) by utilizing self-shunted Josephson junctions (JJs) with critical current density of 600 \( \mu A/\mu m^2 \) and eliminating shunt resistors. This is ultimately small cell using conventional JJ toolbox (SIS JJs, inductors).

• Expanding toolbox – adding ferromagnetic JJs (magnetic JJs, MJJs)
  • All implemented magnetic memories developed during IARPA-funded C3 project are much larger and less energy-efficient due to dominating cell-selector circuits.
    • used SQUIDs
    • used nTrons (hTrons)
  • Using MJJ as a storage element is a good idea (it is non-volatile and very small), but lack of small tri-terminal cell selector negate this advantage

New Memory proposals are appearing:

• Delay-line based memory (Pulsar of G. Tzimpragos) based on high kinetic inductance passive transmission lines

• Mesoscopic superconducting memory based on bistable magnetic textures (Leiden U., TUD)
Memory based on stacked magnetic and Josephson junctions can meet these requirements.

- Can form dense, addressable RAM array (small pitch = memory cell size + safe distance to the next cell)
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- Includes write/erase elements
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Device Structure – Multi-terminal MTJ+SIS device

Schematic view of a four-terminal SIS′F₁IF₂S device and its biasing

SEM micrograph of an actual SIS′F₁IF₂S device

Device Characteristics

$M(H)$ dependence at 10 K for a 5 mm $\times$ 10 mm array of 2 $\mu$m $\times$ 2 $\mu$m pillars made of the same structure as the four-terminal devices. Red dashed lines denote the range of $H$ sweeping in the panel (b).

$I_c(H)$ dependence for the sensor junction in a four-terminal SIS’F$_1$IF$_2$S device while sweeping an external in-plane magnetic field in two opposite directions in the range of $\pm 13.9$ mT after initializing the magnetic state of the device at $\mu_0H + 59$ mT. A significant change in $I_c$ in the range of $\mu_0H \pm 4.5$ mT corresponds to a most significant change in magnetic moment of Py (panel (a)).
Schematic view of a complete memory cell consisting of vertically integrated Superconductor-Insulator-Superconductor (SIS’) and magnetic tunnel junction (MTJ). Pictures show magnetic lines of force for
(a) anti-parallel (AP) magnetization alignment
(b) parallel (P) magnetization alignment (causes suppression of $I_c$).
• Memory array composed of SIS’ F₁IF₂S devices (stacked MTJ and SIS). Independent superconducting control lines with $I_x$, $I_y$ running along the x and y axis, respectively, provide cell selection and switching the magnetization direction of the “soft” magnetic layer in the F₁IF₂ junction (red arrows denote magnetization vectors).
• The SIS’ junctions are connected in series in the rows. $I_r$ is running along the x axis through SIS’ only.
• WRITE operation: Magnetization reversal of the "soft" (bottom F₁) layer is accomplished by combined action of the magnetic field induced by $I_x$ and $I_y$. In the selected cell, the fields from the two lines add up.

• These control lines are insulated from the MTJs and from each other by thin layers of dielectric material (e.g., SiO₂).

• $I_x$ and $I_y$ are flowing through a superconducting path (no energy lost), in contrast to the spin-torque or spin-Hall devices where current flow through highly resistive path.

• WRITE current: the current will depend on the device size. Current $I$ through a thin-film stripe of width $w$ will create the field $H=I/w$. For a device published in PRApp1, if we assume that the remagnetization field is 5 Oe, and the width of the current-carrying stripe producing the magnetic field is 2 um, then I calculate the current to be about 0.8 mA.
**READ operation**

**READ** – reading out local field (not magnetoresistance) through SIS’ critical current change

**READ operation**: \( I_r \) is supplied to the desired row of SIS’ JJs; simultaneously, \( I'_y \) is supplied to the respective column in order to select a cell whose state needs to be read out.

- The magnitude of \( I'_y \) is such that it creates a magnetic field that shifts \( I_c(H) \) along the \( H \) axis but cannot reverse the magnetization in any of the magnetic layers in the MTJ.
- The amplitude of the read current \( I_r \) is chosen as shown by the horizontal line.
- \( I_r \) is flowing through a superconducting path except the selected cell in P orientation (with suppress \( I_c \)) – maximized energy efficiency (energy dissipates when reads “1” only).
Scaling Consideration: Near term options

- In the devices made so far, the SIS’ junction has $j_c \sim 11 \text{ kA/cm}^2$.
- Assume that, upon the size reduction, the maximum Josephson current has to be maintained at about 100 $\mu$A (typical value used in SFQ circuits at 4.2 K); then the SIS’ junction area will be about 0.9 $\mu\text{m}^2$, and the magnetic junction area will be about 0.45 $\mu\text{m}^2$.
- Since both the Josephson coupling energy and the ferromagnetic volume (proportional to the magnetic field) scale in the same proportion (we assume that the film thickness of F1,2 layers is constant), we expect that the relative suppression of $I_c$ for the smaller device will be the same as that for the current devices in the “worst-case” scenario of the stray-field mechanism.
  - since the coercive force typically INCREASES with decreasing the magnetic element size, then, theoretically, one needs a higher remagnetization field. But since $H=I/w$, reducing $w$ will increase $H$ at the same $I$, which makes the situation not so bad. Ultimately, one needs to look for F materials with lower coercive fields. Perhaps alloys may help.
- Optimization of the device parameters will improve the $I_c$ difference for P and AP magnetization orientations and will allow for further size reduction.
  - ~30% suppression has been shown (ISEC 2017)
  - SIS area should be decreased
  - Thickness of middle layer S’ be should decreased
  - Relative position of MTJ over SIS JJ should be optimized.
Comparison to the Requirements

✓ Can form dense, addressable RAM array: Multiple terminals including the terminals to the middle of the stack enable addressable dense memory array integration

✓ Small addressable memory cell (not just small memory element) – stacked storage element (MTJ) and sense circuit (SIS)
   ✓ Includes read/sense elements
   ✓ Includes write/erase elements

✓ WRITE: done by using magnetic field created by two lossless superconducting control lines.

✓ READ: Instead of reading out magnetoresistance of MTJ, we read out the stacked JJ critical current modulated by relative magnetization in MTJ
   ✓ Selecting currents are applied via lossless superconducting lines
   ✓ Does not burn energy in non-selected cells
   ✓ Energy is spent only in the selected cell
   ✓ Reasonable power requirements (i.e. current amplitude) for RAM line drivers

✓ Fast read (in ps) determined by SIS. Moderately fast Write (< 100 ps) determined by MTJ

✓ Manageable Half-select (i.e. can work with individual cell or row without affecting neighboring cells)

✓ Compatible to single flux quantum digital circuits in fabrication signal and speed levels.