

BEST UTILIZATIONS OF LOW-ENERGY HIGH-SPEED ADVANTAGES OF SUPERCONDUCTING LOGIC

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Going Faster with Less Energy

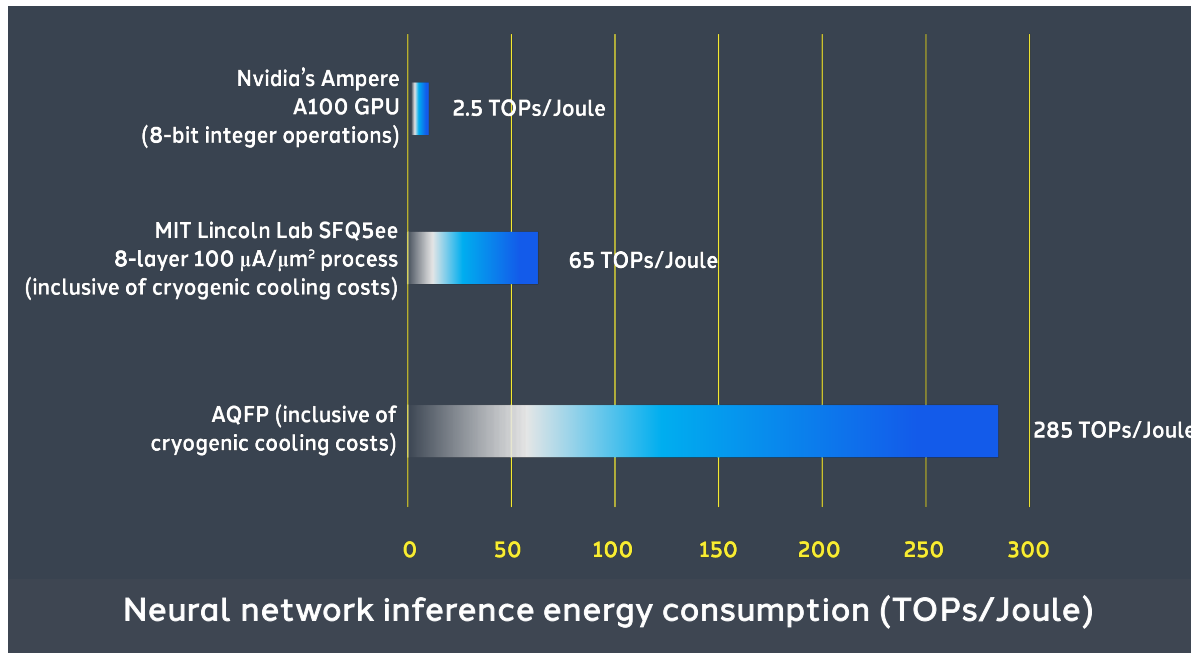
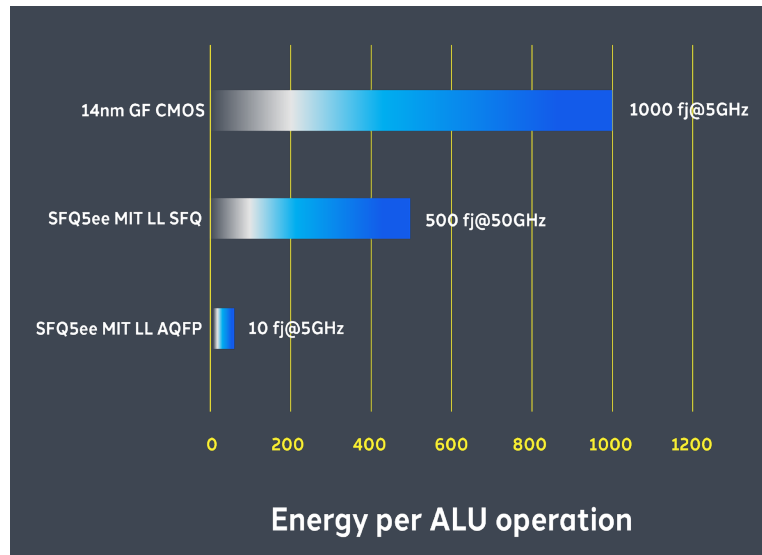
- Very high clock frequencies
 - High single-threaded performance through short switching times and fast signal propagation
- Ultra low switching energy
 - Energy related to the generation of the bit information should be made as small as possible

Superconductor circuits meet both of the aforesaid requirements and have become a strong candidate for a beyond-CMOS computing fabric. This technology is known for the high clock frequencies, 2–50 GHz, and the low energy dissipation per logical operation, down to several zJ [1].

[1] K. K. Likharev and V. K. Semenov, RSFQ logic/memory family: A new Josephson-junction technology for sub-terahertz-clock-frequency digital systems, *IEEE Trans. Appl. Supercond.* 1, 3 (1991).

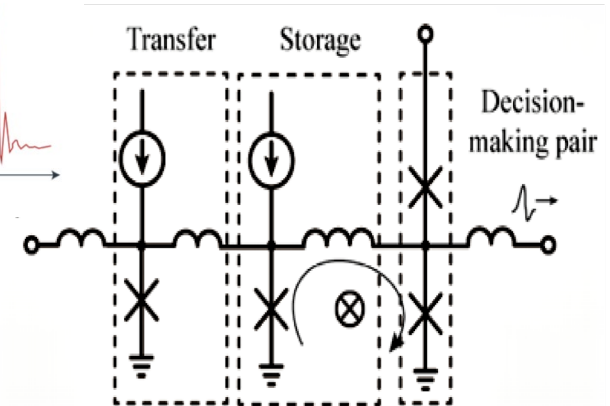
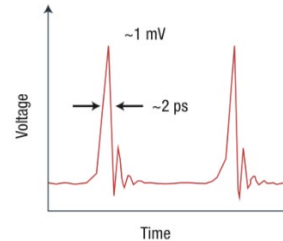
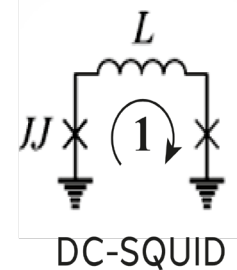
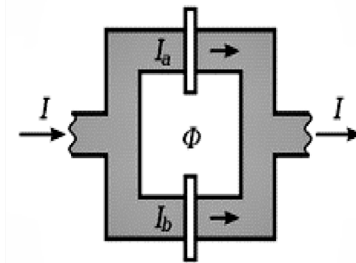
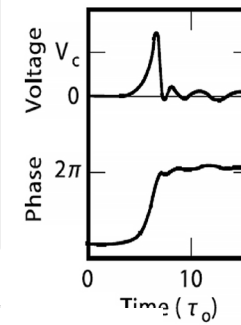
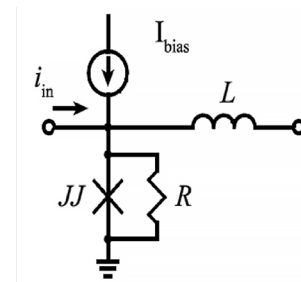
[2] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, Measurement of 10zJ energy dissipation of adiabatic quantum flux-parametron logic using a superconducting resonator, *Appl. Phys. Lett.* 102, 052602 (2013).

Case for Superconductor Circuits



Single Flux Quantum (SFQ) Logic

- **Pulse-based logic family**, inherently synchronous, limited fanout drive
- Basic element of RSFQ logic is superconducting loop interrupted by one or more JJs
 - If the loop inductance L is high enough such that $I_C L \geq \Phi_0$, then SFQ can be held in the loop as a **persistent current representing logical one**, whereas an **absence of SFQ means logical zero**
 - Magnetic flux ejected from a superconducting loop through a JJ takes the form of **tiny voltage pulses** (mV, ps)
- Building blocks of SFQ circuits
 - **Transfer and storage sections**
 - **Decision-making pairs**



Unique Characteristics of SFQ Logic

Different active and passive components

- Two-terminal JJ's and inductors vs. 3-terminal transistors and capacitors in CMOS

Superconducting interconnect

- Josephson transmission lines (JTLs) and passive transmission lines with small series resistors to prevent flux storage (PTLs) vs. lossy interconnect in CMOS

Different suites of basic cells

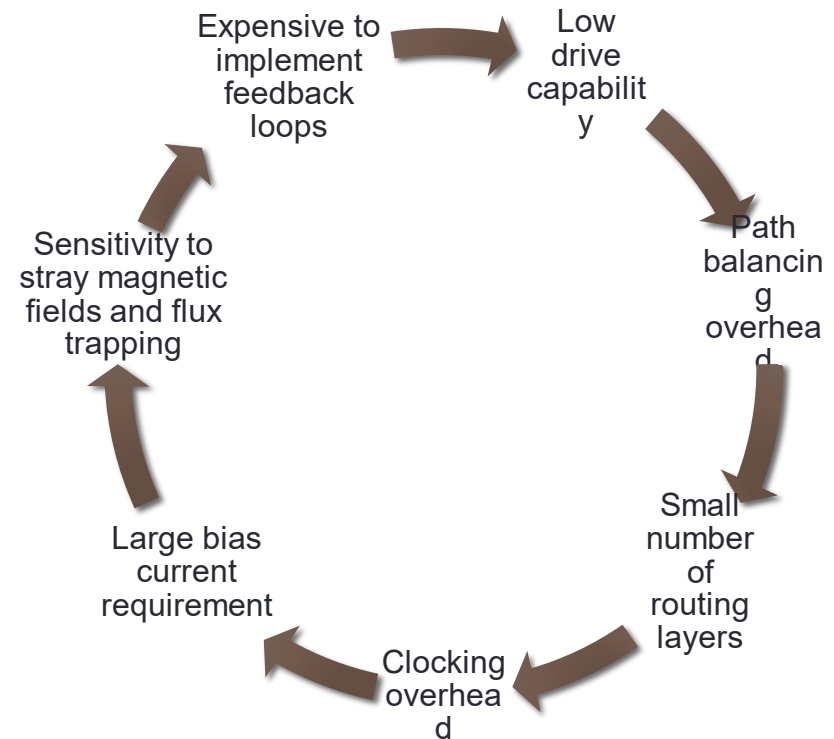
- Simple clocked cells (NOT, AND, OR, XOR, DFF, NDRO) and some clockless cells (delay cells, splitters) vs. complex multi-input logic cells in CMOS

The RSFQ main advantage driving its development has been the high speed at very low overall power consumption.

Major disadvantage has been the large SQUID cell size severely limiting the integration level.

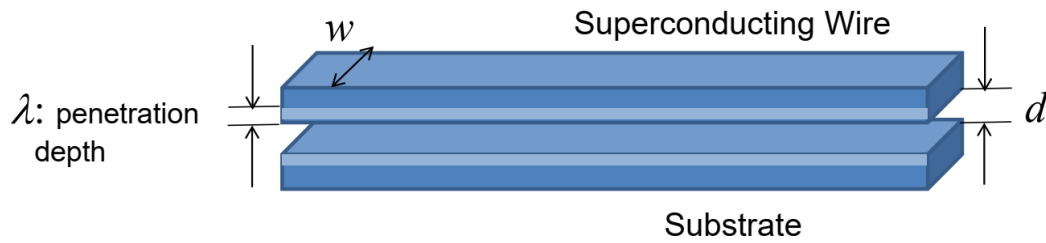
Furthermore, the parallel bias lines carry high currents, and associated magnetic fields must be shielded, which is difficult.

The clock network requires a significant overhead in JJs number.



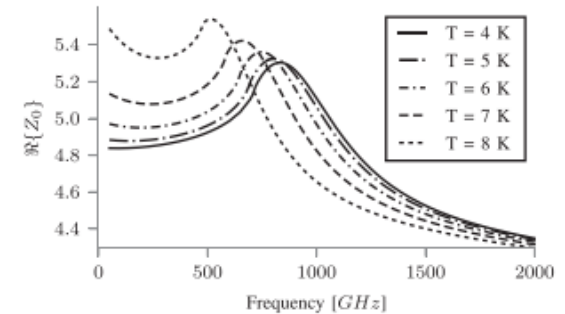
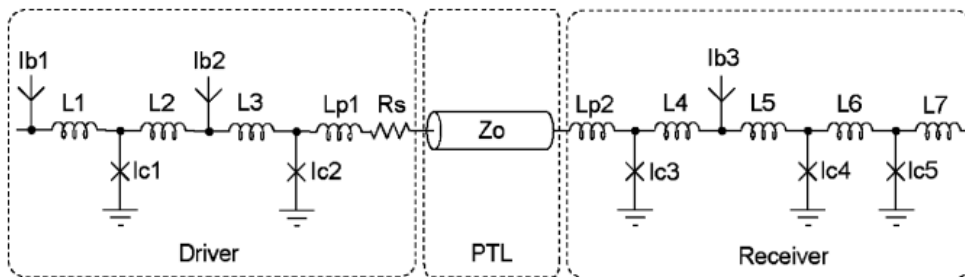
Circuit-Level Challenges

Advantage: Passive Transmission Lines



$$v \cong \frac{1}{\sqrt{\epsilon\mu(1 + 2\lambda/d)}}$$

@ 100GHz, T=5K:
 50 nH/m
 100 Ω /m
 0.34 speed of light



- Superconducting transmission is dispersion free, i.e., we have **ballistic propagation of an SFQ pulse** [5]
- Speeds up to 1/3 of the speed of light are achieved (**Typical delay: 10 ps/mm**)
- Needs PTL driver and receiver circuits, **Delay scales linearly with PTL length** [6].
- Must be impedance matched to the JJs of driver and receiver circuits. Junctions in the latest fabrication processes allow about 5 to 10 Ω lines, which reduces line width for tighter integration.

PTLs are a highly appealing feature in RSFQ circuits.

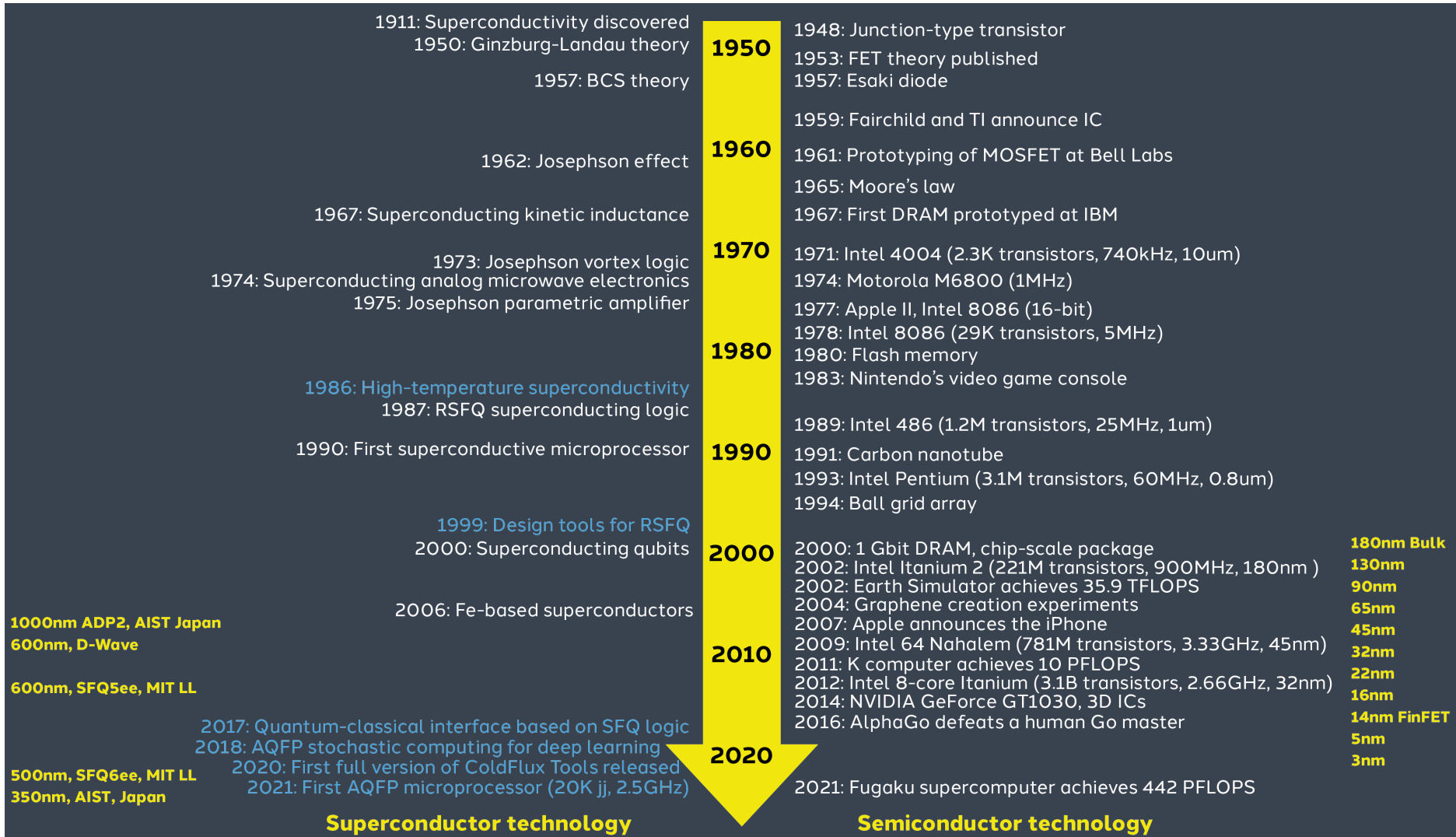
[5] Takagi, Katsumi, et al. "SFQ propagation properties in passive transmission lines based on a 10-Nb-layer structure." *IEEE Transactions on Applied Superconductivity* 19.3 (2009): 617-620.

[6] P. I. Roux, K. Jackman, J. A. Delport and C. J. Fourie, "Modeling of Superconducting Passive Transmission Lines," in *IEEE Transactions on Applied Superconductivity*, vol. 29, no. 5, pp. 1-5, Aug. 2019, Art no. 1101605.

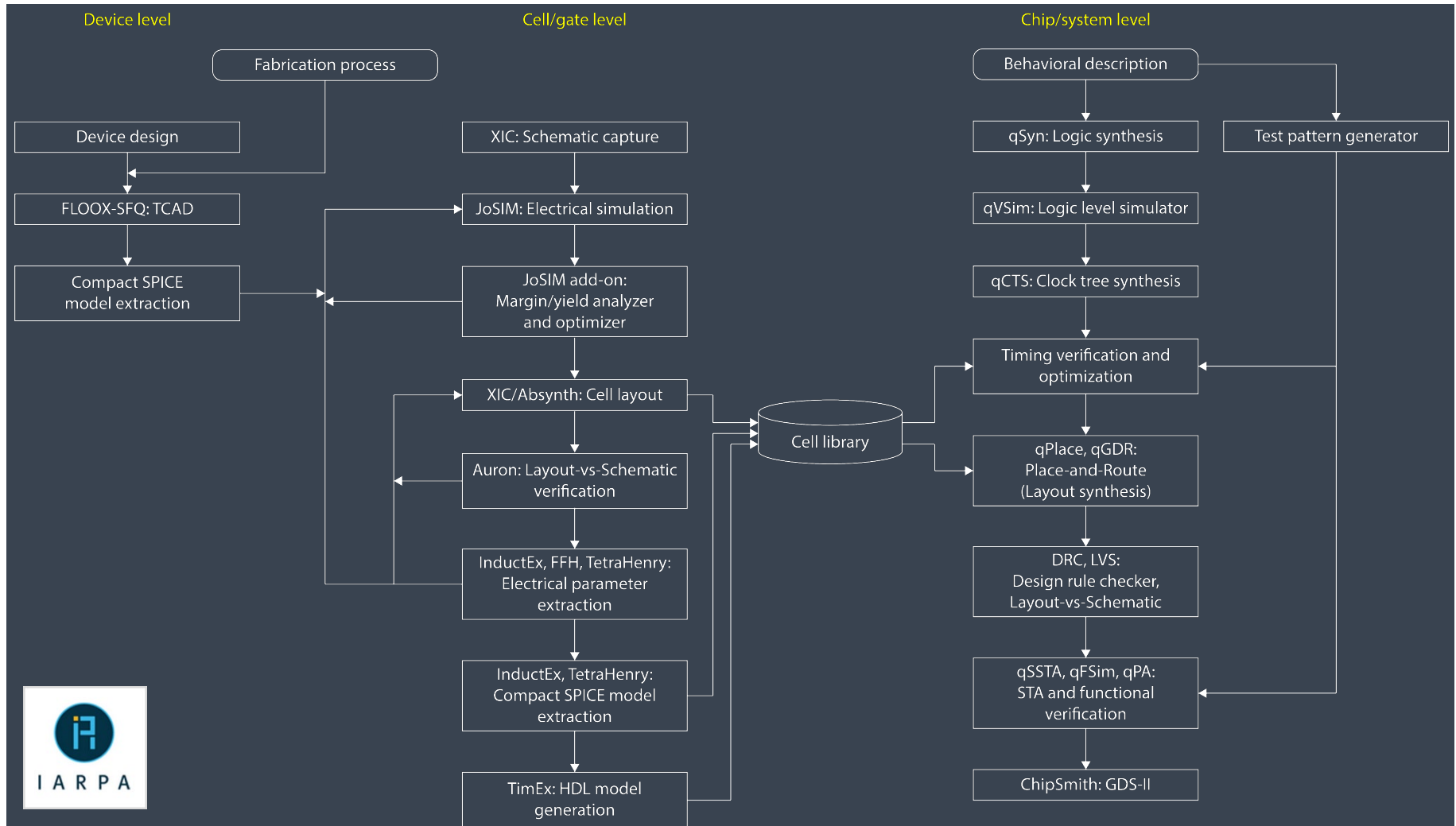
SFQ Challenges and Potential Solutions

TECHNICAL CHALLENGES AND OPEN PROBLEMS	Socioeconomic impacts			
	Languages, compilers, and runtimes	Economic impact	Climate/ environmental impact	Statistical and data analytics methods
	Architecture and multi-threading	SuperSoCC design		
	Interfaces across temperature zones and technologies	Superconductive MCM	Application optimization and mapping	Software stack development
	Current delivery, clocking, and synchronization	Integration and interfaces		
	Dense on-chip memory	Electrical-thermal-mechanical optimization	Passive and active integration technologies	Cables, clocks, and bias lines
	Stray electromagnetic fields	Circuits and architecture		
Physical scaling and integration	Multi-bit SFQ and temporal logic circuits	All-JJ, 2ϕ -JJ, and DSFQ logic	Dual clocking, current recycling, and power biasing	
	Devices and materials			
	Nanowire devices e.g., nTron, QPSJ	Bistable magnetic JJs	Superconducting ferromagnetic transistors	

Story of Two Timelines

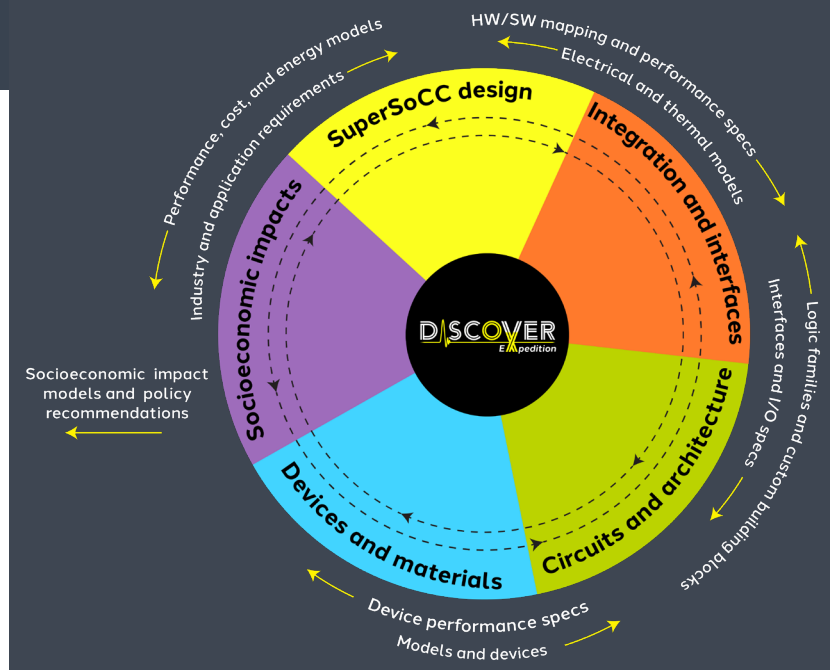
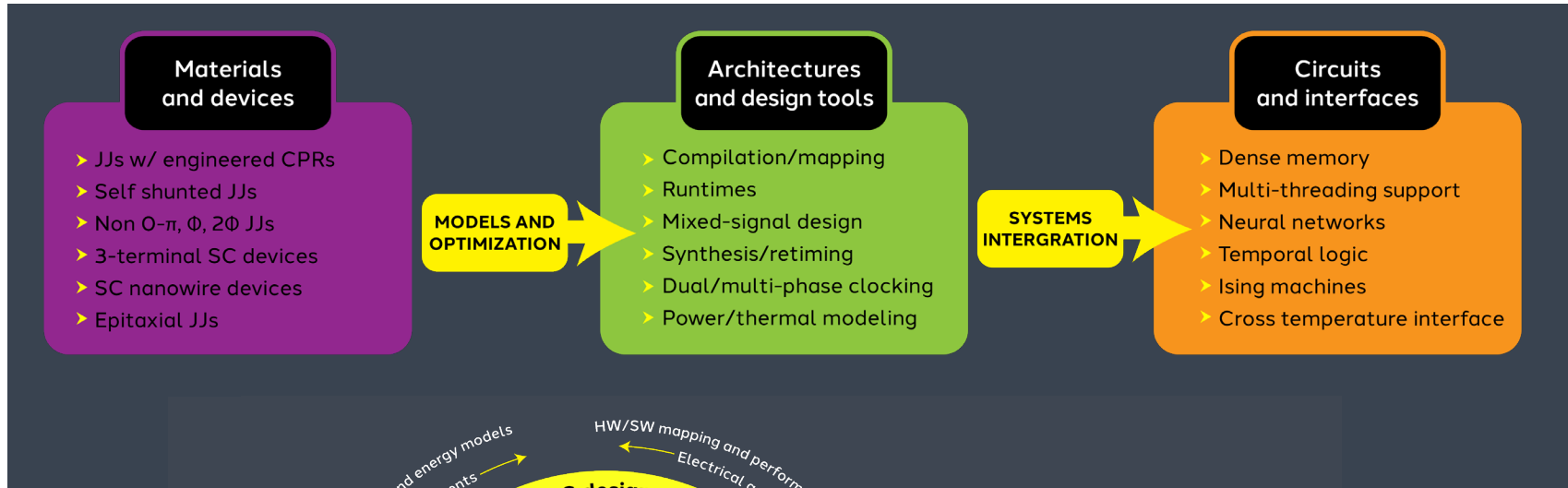


IARPA SuperTools Program: ColdFlux Tools



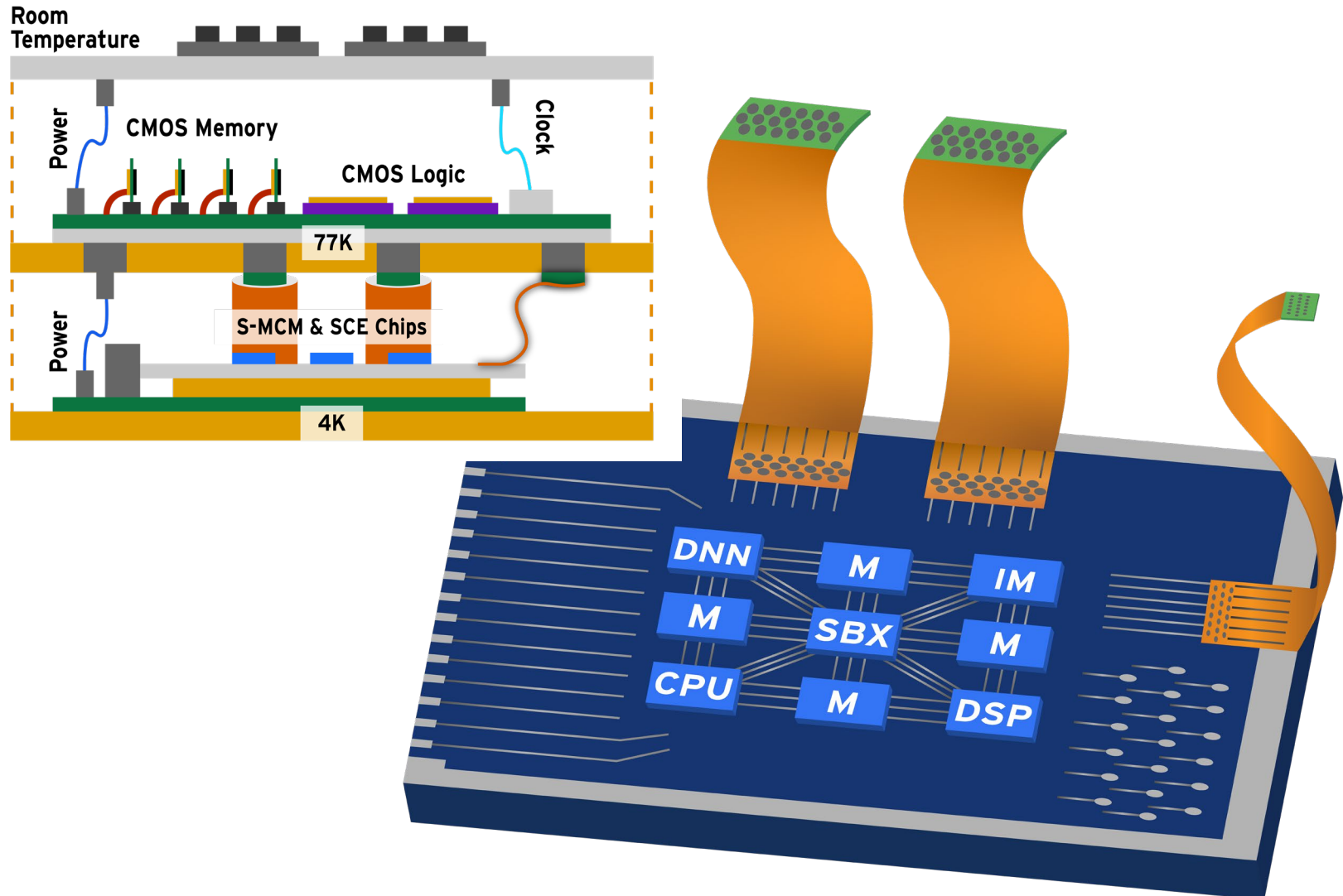
NSF DISCoVER Expedition

Design & Integration of Superconductive Computation For Ventures beyond Exascale Realization



<https://discoverexpedition.usc.edu/>

SFQ-Based Multi-Function Accelerator



Characteristics of Computing Applications Suitable for Superconductor Electronics

- The problem has usually been the cost of the superconducting versus non-superconducting solutions.
 - Future successes in reducing the cost, size, weight, unreliability, etc. of cryogenic equipment will have a direct and strong impact on how quickly various applications can be commercialized
- Computing applications: Feedforward pipelined architectures with minimum stalls and pipeline flushes
- Other applications: Benefit from features such as voltage-controlled oscillation, fast digital-to-analog conversion, operation at ultracold temperatures, true random number generation, etc.

Common Applications

- In electronics, the Josephson effect has enabled devices such as SQUIDs (superconducting quantum interference devices) for the most accurate measurement of magnetic fields, voltage (e.g., the Josephson Voltage Standard), and related electromagnetic quantities
- Researchers have also experimented with SQUID RF amplifiers, superconducting low-inductance undulating galvanometer (SLUG), SQUID magnetometers (with flux-locked feedback loops), Josephson parametric oscillator, and A/D converters.
- In addition to the magnetic resonance imaging, one of the largest commercial use at present of superconducting electronic devices (HTS) is as filters in cell phone base stations.
- Superconductors are also used for the highest Q resonant cavities, particularly in high-energy particle accelerators.

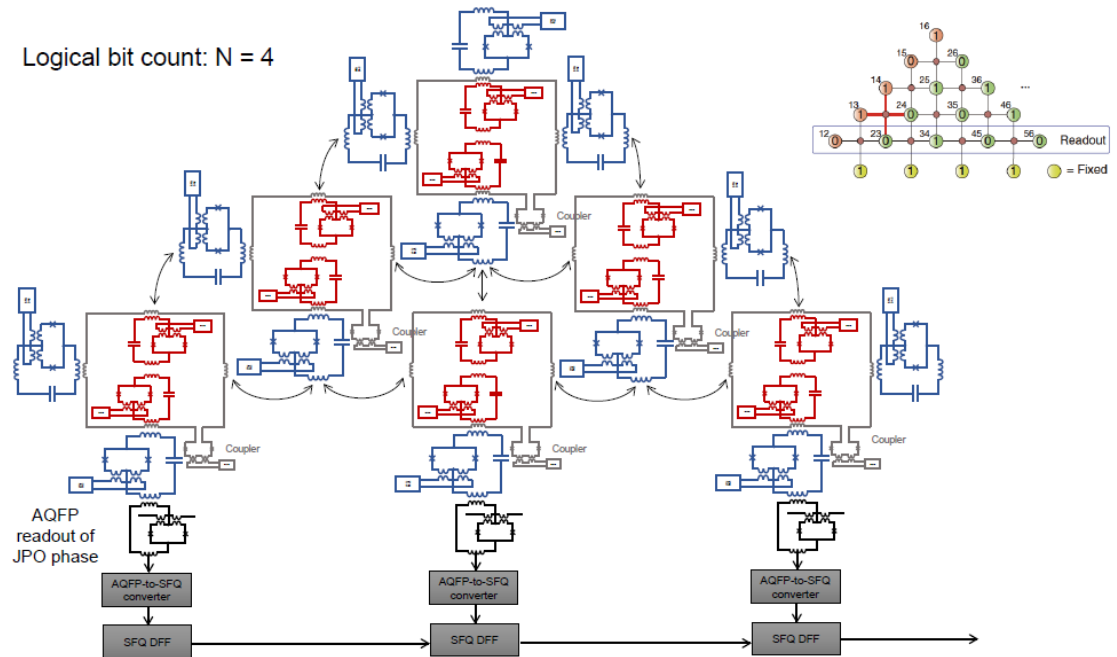
Ising Hamiltonian solver based on Josephson parametric oscillators

- Adiabatic annealing involves the encoding of an optimization problem using the interactions between classical variables that can take the values ± 1 .
- The combinatorial optimization problem is then cast in the form of an all-to-all Ising spin glass model:

$$\mathcal{H} = \sum_{i,j < i} J_{ij} \sigma_i \sigma_j + \sum_i h_i \sigma_i$$

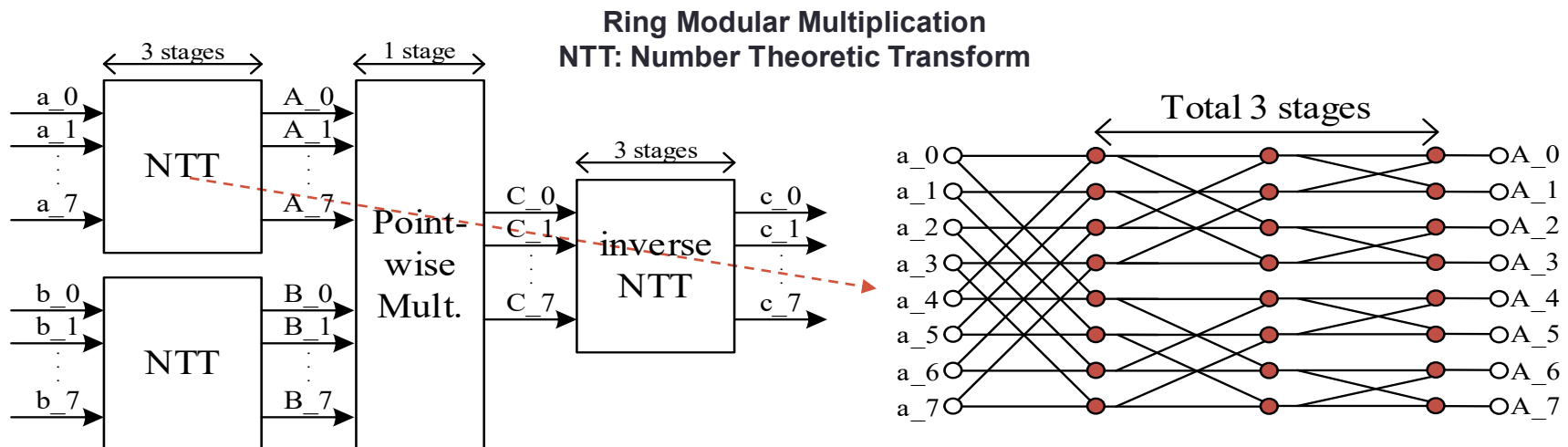
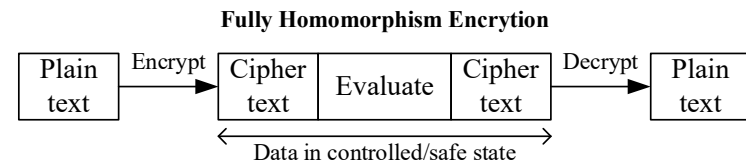
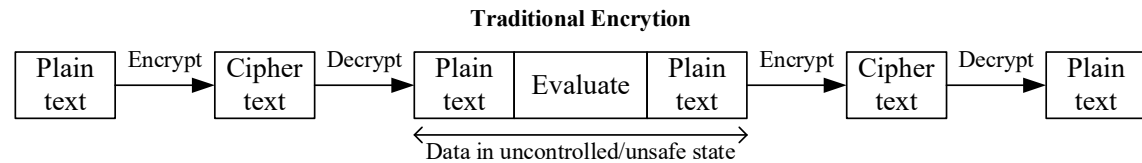
where $\sigma_i \in \{-1, +1\}$ represents the i^{th} spin.

- The interaction matrix J_{ij} and the additional local magnetic fields h_i fully parameterize the optimization problem.
- The task of finding the optimal solution amounts to finding the ground state of \mathcal{H} .

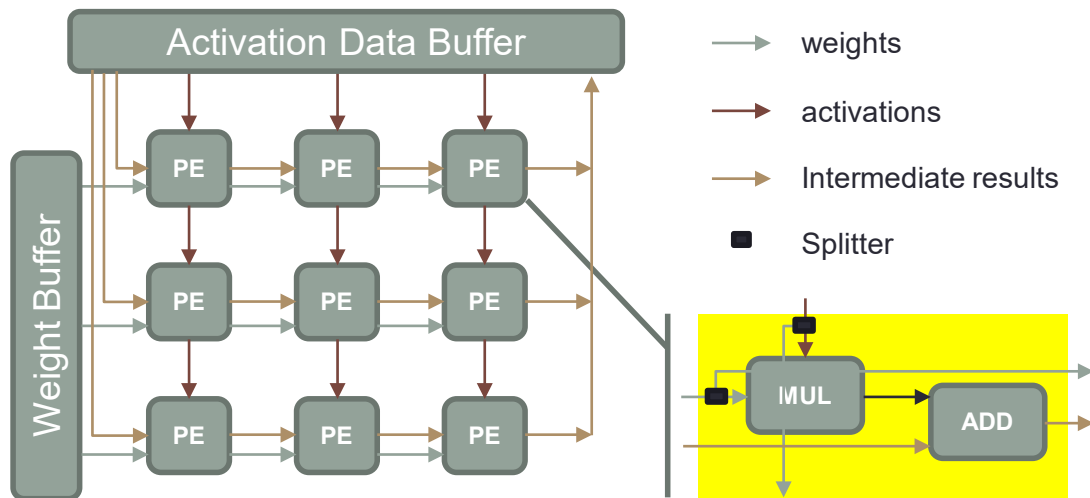
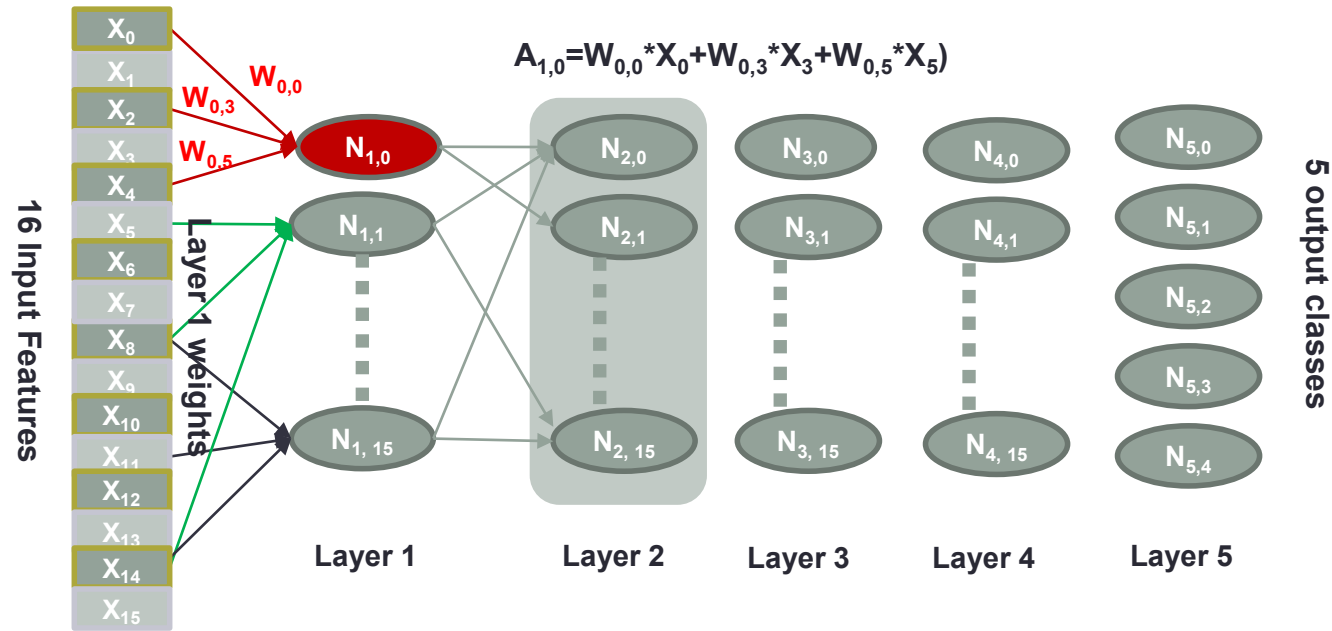


Fully Homomorphic Computation

- FHE schemes use these two primary parameters to tune the provided security and the supported depth of homomorphic computation.
- Example values of n and $\log_2(q)$ are 4,096 and 1,024, respectively.
- The challenge comes from the difficulty of supporting both a large ring dimension n (which provides comparatively better security) and a large $\log_2(q)$ (which increases the depth of supported computations).



Neural Network Acceleration

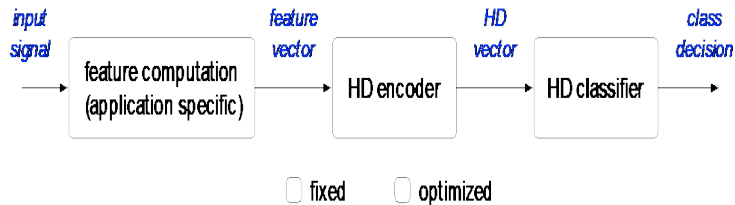


Hyperdimensional Computing

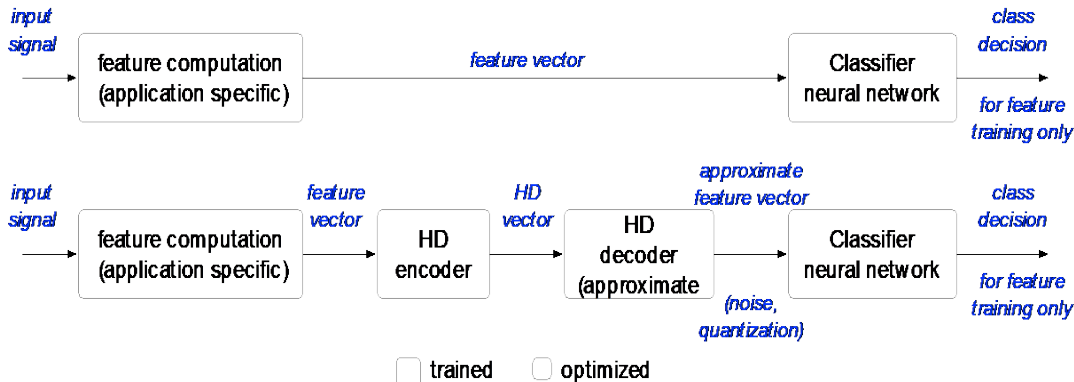
Standard HD classification system are comprised of three components:

1. Input feature extractor mapping input signal to a feature vector
2. HD encoder maps low-dimensional feature vector into HD vector
3. HD classifier maps HD vector into a classification decision

Unfortunately, feature computation is highly application specific, **not trained as part of design, and highly compute-intensive** thus dominating the HD processing complexity and thus overall system complexity.

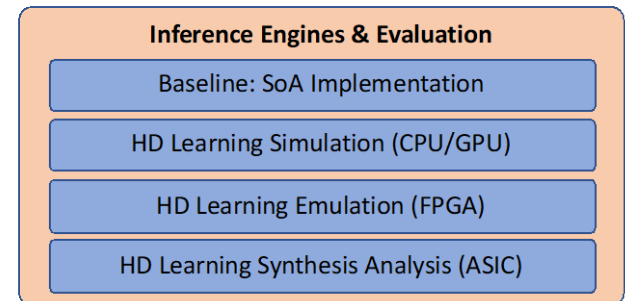
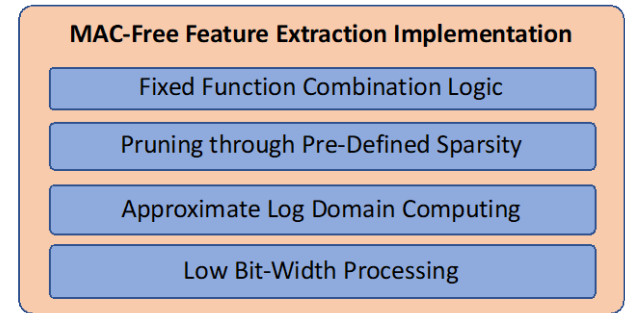
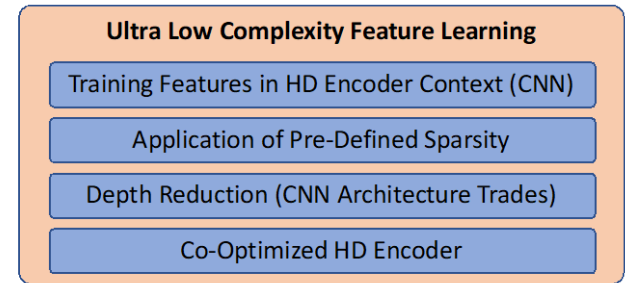


Standard Processing for Hyper-Dimensional Classification



HD Learning's Approach for feature computation for dataset and application

Application, Library, Datasets Inputs

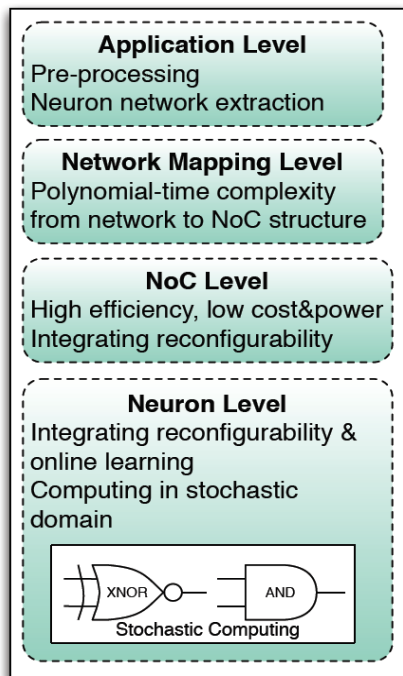


Results {Performance, Accuracy, Latency}

Stochastic Computing

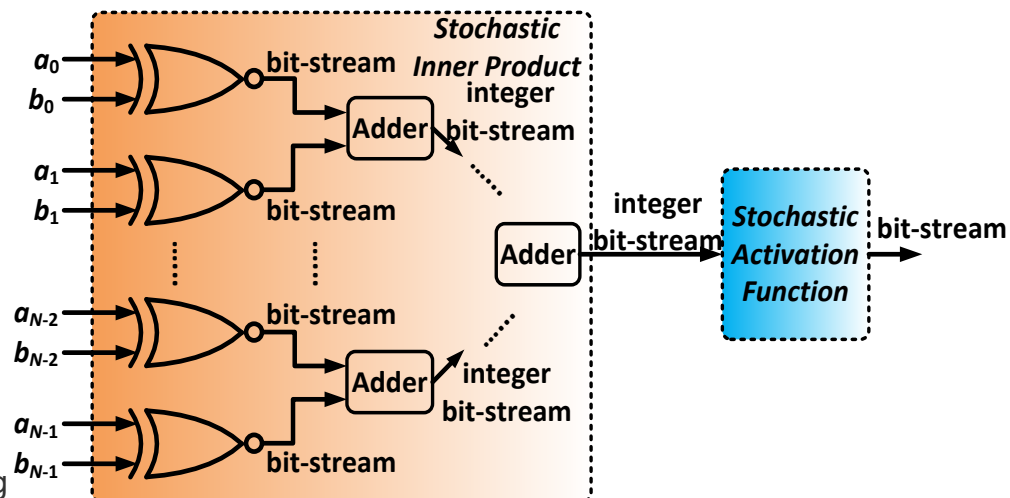
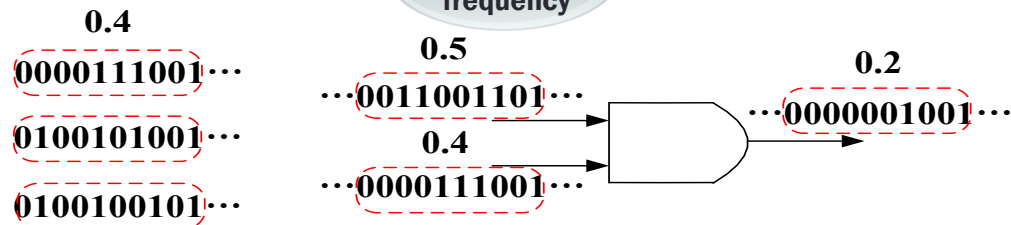
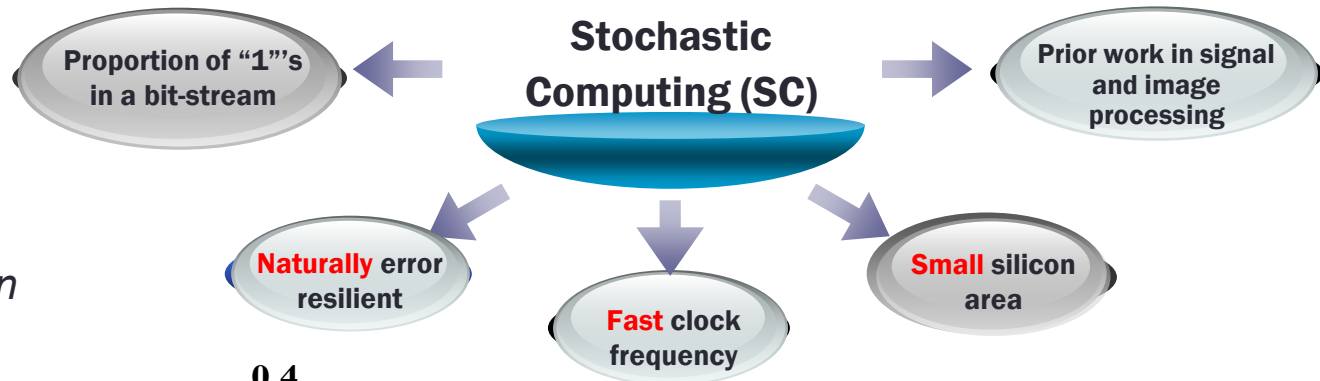
One can use stochastic computing to realize key computational blocks of neurons, e.g., *inner product calculation, pooling, normalization, and activation function application.*

Overall Framework



Evaluation & Validation

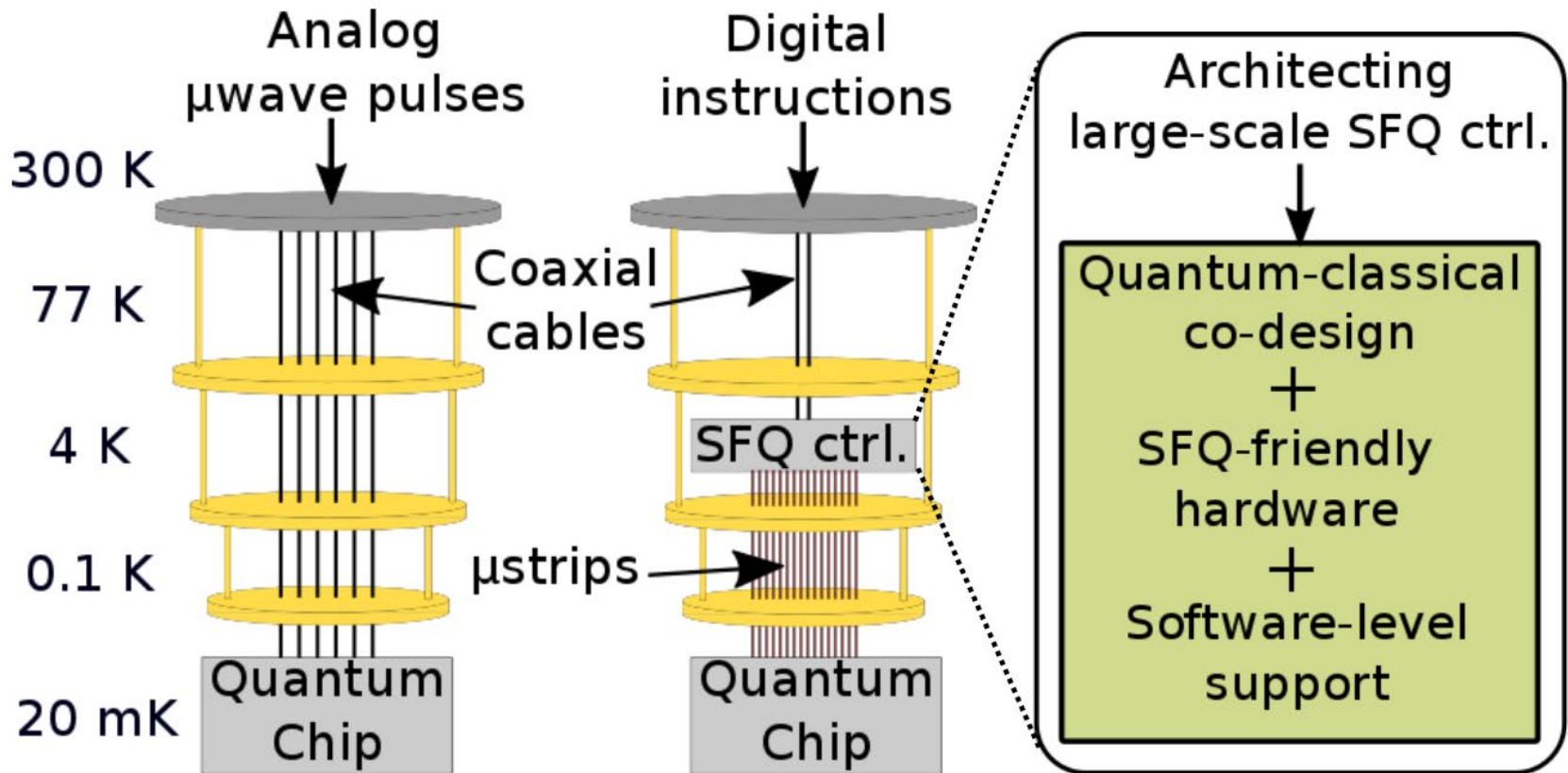
Characteristics
 High-scalability
 Low power
 High resiliency
 High performance
 Reconfigurability
 Online training capability



SC Example: Inner Product Calculation

R. Cai *et al.*, "A Stochastic-Computing based Deep Learning Framework using Adiabatic Quantum-Flux-Parametron Superconducting Technology," 2019 ISCA, pp. 567-578.

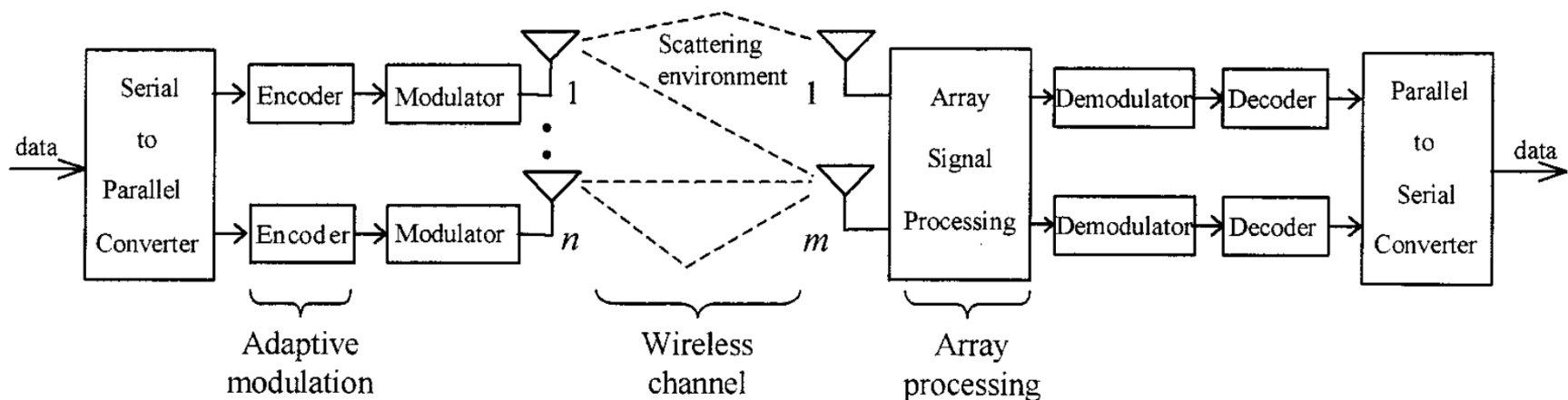
Error Correction and Control of Quantum Computers



M.R. Jokar, R. Rines, G. Pasandi, H. Cong, A. Holmes, Y. Shi, M. Pedram, and F.T. Chong, "DigiQ: A Scalable Digital Controller for Quantum Computers Using SFQ Logic," In *Int'l Symp. on High-Performance Computer Architecture*, 2022: 400-414.

Array Signal Processing for Millimeter Wave Communications

Massive MIMO systems can generate potentially prohibitive amounts of data due to the large numbers of antennas. With modern parallel, low-rate analog-to-digital converters (ADCs), the bottleneck is often not in the quantization of the received signals but, rather, in the processing of the digitized bits.



To separate the n transmitted signals in the receiver, a commonly used scheme linearly combines the received signals using a set of weights that yields the minimum mean square error (MMSE) between the detected data and the true signal samples

Conclusion

- Because of the cryogenic burden, new superconducting applications are most likely to achieve early, widespread success in situations where there are clear performance and energy efficiency advantages.
- In spite of much progress in SCE, key challenges exist in way of physical scaling, controlling stray electromagnetic fields, supporting multiple clocks, current recycling, design centering to improve operating margins, designing dense on-chip memory, etc.