Optimization of Suzuki Stack Circuit to Reduce Power Dissipation

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Optimization of Suzuki Stack Circuit to Reduce Power Dissipation

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Abstract—Superconductor–semiconductor hybrid circuits can combine the benefits of the high-speed and low-power operation of single-flux quantum circuits and high integration densities of CMOS technology such as memory. The Suzuki stack, a type of Josephson latching driver/amplifier, is a widely used interface circuit in Josephson–CMOS hybrid memories. Due to the limited cooling power at cryogenic temperatures, the power dissipation is becoming an important concern, especially in large-scale systems. An optimization technique to significantly reduce the power dissipation of Suzuki stack circuits is proposed in this article. The proposed design can reduce the power dissipation by 30–70% while causing a voltage drop of 2–9% in the output voltage depending on the circuit parameter configuration. The tradeoffs between the power dissipation and output voltage characteristics are discussed. The proposed design can operate correctly within at least ±20% of process parameter variations as demonstrated with extensive simulations.

Index Terms—Suzuki stack circuit, Josephson latching driver/amplifier, Josephson–CMOS memory, superconductor–semiconductor interface circuits, power dissipation.

A Josephson–CMOS hybrid memory uses the Suzuki stack and CMOS amplifier circuits to convert SFQ pulses to CMOS-level voltage signals. For instance, a 64-kb hybrid Josephson–CMOS random access memory (RAM) operating at 4 K has been demonstrated in [9]. In this system, the Suzuki stack circuit is designed to produce the output voltage of 60 mV, with an average power dissipation of 165 \( \mu \)W. The 12-b address inputs, one read, one write, and 16-b data inputs are required to access the 64-kb RAM. As a result, 30 Suzuki stack circuits are needed (i.e., one for each input signal). During the read and write operations, Suzuki stack circuits dissipate 2.31 mW and 4.95 mW, which corresponds to 19.5% and 23.6% of total read and write power, respectively. At 4.2 K, the cooling power is limited to around 1–1.5 W [14], [15], depending on the size of the cryostat. In large-scale systems (e.g., data centers and cloud computing), the improvement in power dissipation in order of tens of milliwatt becomes highly important. For example, Konno et al. [16] have proposed a technique to reduce the power dissipa-
About me

• 2nd year PhD student studying at Department of Electrical and Computer Engineering
• Advisor: Prof. Selçuk Köse
• Research interests:
  • Superconducting electronics
  • Superconductor-semiconductor interface circuits
  • Hardware security
• Currently working as an intern at SeeQC (Elmsford, NY)
  • Cryogenic testing and analysis of superconducting integrated circuits, fabrication diagnostics
Outline

1. Background
2. Motivation
3. Proposed optimization technique
4. Conclusions
5. Overview of current research
Outline

1. Background
   a. Underdamped Josephson junctions
   b. Suzuki stack circuits

2. Motivation

3. Proposed optimization technique

4. Conclusions

5. Overview of current research
Underdamped Josephson Junctions

- **Stewart-McCumber parameter:**
  \[ \beta_c = \frac{2\pi}{\Phi_0} I_c R^2 C_J \]
- Underdamped: \( \beta_c \gg 1 \)
- Widely used in latching logic back in 1980-90s
- Hysteric behavior
- Simulated I-V characteristics for MIT-LL SFQ5ee 10 kA/cm\(^2\) process
- Shunt resistance:
  \[ R_{Sh} = 6V_g/I_c \]

Suzuki Stack Circuits

- Josephson latching driver, superconductor-semiconductor interface circuit
- Can convert SFQ pulses to tens of mV DC signal
- Used in Josephson-CMOS hybrid memory
- Ideal output voltage = $N V_g$
- Compared to SQUID stack and SFQ-to-DC converter:
  - Higher output voltage
  - Smaller area (few JJs)
  - Faster operation

Suzuki Stack Circuits
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Motivation

• Limited cooling power in large-scale systems (1-1.5 W at 4.2 K)
• Single Suzuki stack cell dissipates 165 µW
• 64-kb Josephson-CMOS RAM consists of 30 Suzuki stack cells
  • 2.31 mW (read) and 4.95 mW (write)
  • 19.5% and 23.6% of total read and write power

• Objective: reduce power dissipation in Suzuki stack circuit
  • Reducing bias current
  • Using non-equal critical current values of JJs
Outline

1. Background
2. Motivation
3. Proposed optimization technique
   a. Proposed conditions
   b. Analysis of circuit parameter configurations
   c. Simulation results
   d. Margins
4. Conclusions
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Proposed Conditions

• Assumption: ±20% minimum margins

• Conditions:
  1. \( I_l \leq 0.8 \times I_{c,l} \)
  2. \( 1.2 \times I_{c,l} \leq I_{in} + I_l \)
  3. \( 0.8 \times I_b \geq I_{c,r} \)

• Condition #3 reduces power dissipation
  • Original design (biasing to 80% of \( I_c \)):
    \( I_b \approx I_l + I_r \approx 0.8 \times 2 \times I_{c,r} = 1.6 \times I_{c,r} \)

Analysis of Circuit Parameter Configurations

• From conditions #1 and #2, $I_{c,l} = 350 \mu A$ and $I_l = 280 \mu A$

• For $\frac{I_l}{I_b} = a$,
  • $V_b = I_b R_b = \frac{I_l R_b}{a}$
  • $I_{c,r} = 0.8 \times I_b = 0.8 \times \frac{I_l}{a}$
  • $R_l = \frac{I_r}{I_b} \times R_{tot} = (1 - a)R_{tot}$
  • $R_r = R_{tot} - R_l = aR_{tot}$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Original from [22]</th>
<th>$\frac{I_l}{I_b} = 0.50$</th>
<th>$\frac{I_l}{I_b} = 0.55$</th>
<th>$\frac{I_l}{I_b} = 0.60$</th>
<th>$\frac{I_l}{I_b} = 0.65$</th>
<th>$\frac{I_l}{I_b} = 0.70$</th>
<th>$\frac{I_l}{I_b} = 0.75$</th>
<th>$\frac{I_l}{I_b} = 0.80$</th>
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</thead>
<tbody>
<tr>
<td>Bias voltage $V_b$</td>
<td>500.0 mV</td>
<td>420.0 mV</td>
<td>381.8 mV</td>
<td>350.0 mV</td>
<td>323.1 mV</td>
<td>300.0 mV</td>
<td>280.0 mV</td>
<td>262.5 mV</td>
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<td>Left branch resistance $R_l$</td>
<td>4.0 $\Omega$</td>
<td>4.0 $\Omega$</td>
<td>3.6 $\Omega$</td>
<td>3.2 $\Omega$</td>
<td>2.8 $\Omega$</td>
<td>2.4 $\Omega$</td>
<td>2.0 $\Omega$</td>
<td>1.6 $\Omega$</td>
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<tr>
<td>Right branch resistance $R_r$</td>
<td>4.0 $\Omega$</td>
<td>4.0 $\Omega$</td>
<td>4.4 $\Omega$</td>
<td>4.8 $\Omega$</td>
<td>5.2 $\Omega$</td>
<td>5.6 $\Omega$</td>
<td>6.0 $\Omega$</td>
<td>6.4 $\Omega$</td>
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<tr>
<td>Left branch critical current $I_{c,l}$</td>
<td>400 $\mu A$</td>
<td>350 $\mu A$</td>
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<tr>
<td>Right branch critical current $I_{c,r}$</td>
<td>400 $\mu A$</td>
<td>448 $\mu A$</td>
<td>407 $\mu A$</td>
<td>373 $\mu A$</td>
<td>344 $\mu A$</td>
<td>320 $\mu A$</td>
<td>298 $\mu A$</td>
<td>280 $\mu A$</td>
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<td>Left shunt resistance $R_{sh,l}$</td>
<td>42.0 $\Omega$</td>
<td>48.0 $\Omega$</td>
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<td>60.0 $\Omega$</td>
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<td>Parasitic series inductance of JJ</td>
<td>0.13 pH</td>
<td>*</td>
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<td>Bias resistance $R_b$</td>
<td>750 $\Omega$</td>
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<td>Bias inductance $L_b$</td>
<td>200 pH</td>
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<td>Input voltage $V_{in}$</td>
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<td>Input resistance $R_{in}$</td>
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<td>Output resistance $R_{out}$</td>
<td>50 $\Omega$</td>
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<tr>
<td>Output inductance $L_{out}$</td>
<td>100 pH</td>
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<tr>
<td>Output capacitance $C_{out}$</td>
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Simulation Results

• There is a trade-off between power dissipation and output voltage characteristics

• Circuit designer can select parameters depending on given constraints
Margins

• Designs with lower power dissipation are **not degraded** as compared to original design

• Initial assumption is satisfied

• Conditions:
  1. $I_l \leq 0.8 \times I_{c,l}$
  2. $1.2 \times I_{c,l} \leq I_{in} + I_l$
  3. $0.8 \times I_b \geq I_{c,r}$
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1. Background
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Conclusions

• Optimization technique that reduces power dissipation of Suzuki stack circuit is proposed
• Set of design conditions are defined
• Depending on circuit parameter configuration, the power dissipation can be decreased by 30-70%, while reducing the output voltage by 2-9%
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Suzuki Stack Circuit with Differential Output

- Conventional Suzuki stack designs use single-ended output
- Proposed **differential** design provides:
  - Two times larger output voltage swing
  - Better noise immunity
  - Similar operating margins
Questions?

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