DISCoVER Expedition

Design and Integration of Superconductive Computation for Ventures beyond Exascale Realization.

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Design and Integration of Superconductive Computation for Ventures beyond Exascale Realization
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Discovery team

Prof. Massoud Pedram (Director)

Prof. Eby Friedman (Associate Director and thrust leader)

Prof. Murali Annavaram (Thrust leader)

Prof. Grace Xing (Thrust Leader)

Prof. Michael Hamilton (Thrust Leader)

Prof. Ivan Petrovich Nevirkovets

Prof. Julia Albright

Prof. Mark Bocko

Prof. Oleg Mukhanov

Prof. Selcuk Kose

Prof. Yanzhi Wang

Prof. Roman Sobolewski

Prof. Timothy Pinkston

Prof. Nobuyuki Yoshikawa

Prof. Christopher Ayala

USC Viterbi
School of Engineering
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**Thrusts and teams**

**Thrust 1: SuperSoCC Design (Lead: Annavaram)**
- Design the SuperSoCC-I and SuperSoCC-II
- Superconducting Multi-chip module architectures
- Adapting RISC-V tools for SuperSoCC

**Thrust 2: Circuits and Architecture (Lead: Friedman)**
- Demonstrate the SuperSoCC
- Develop novel circuits and architectures
- Design techniques and VLSI
- Superconductor memory

**Thrust 3: Devices and Materials (Lead: Xing)**
- Novel materials for π-JJs and 2φ-JJs for addressing memory and scaling issue.
- New devices and CAD tools and models for them.

**Thrust 4: Integration and Interfacing (Lead: Hamilton)**
- MCM Interface and Integration
- Low loss and low latency room temperature (>77K) to cryogenic interface.
- Connector and wiring models for 4K

**Thrust 5: Business and Socioeconomic Impacts (Temporary Lead: Razmkhah)**
- Social impacts
- Economic impacts
- Environmental impacts
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Thrusts and teams (Technical)

- π-Josephson junctions (π-JJs) and 2ϕ-JJs
- three terminal operation of memory through
- ferromagnetic transistors
- cryogenic spin transfer magnetic memory
- quantum phase slip junctions

- multi-bit SFQ storage cells
- multi-valued dynamic SFQ logic fabrics
- (VLSI) complexity
- Current, biasing, clocking,
- thermal gradients, stray magnetic fields

- MCM
- High speed thermal isolated cables
- data movement technologies
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Main Challenges

• **Scaling and Density**: Increasing current density and self shunted junctions.

• **Fanout and Latency**: microarchitecture techniques, clustered ALUs and hierarchical scheduling

• **Ultra-deep Pipeline Structure**: Use of self clocked cells and DSFQ

• **Interface with Room Temperature**: multi-chip modules, design interfaces for efficient SFQ-to-DC or SFQ-to-CMOS conversion, Low loss ribbon wiring.

• **High Current Bias**: Current recycling and change of architecture.

• **Catch Memory and RAM**: New dense memory architecture design.
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### Year 1 and 2 tasks

<table>
<thead>
<tr>
<th>Thrusts</th>
<th>Y1-Q1</th>
<th>Y1-Q2</th>
<th>Y1-Q3</th>
<th>Y1-Q4</th>
<th>Y2-Q1</th>
<th>Y2-Q2</th>
<th>Y2-Q3</th>
<th>Y2-Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>T1: SuperSoCC</strong></td>
<td>T1-1 SuperCPU Design</td>
<td></td>
<td>T1-2 SuperDNN Design</td>
<td>T1-3 SuperIM Design</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>T2: Circuits and architectures</strong></td>
<td>T2-1 Setting up the tool flow and design methodology</td>
<td>T2-2 Current recycling tool development</td>
<td>T2-3 Dual and multi-phase clocking tool development and PTL design</td>
<td>T2-4 Bias line distribution and power grid connections</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>T3 Materials and Devices</strong></td>
<td>T3-1 TCAD and compact circuit models for π and 2π JJs</td>
<td>T3-2 TCAD and compact circuit models for nanowire devices</td>
<td>T3-3 TCAD and compact circuit models for proposed memory cell</td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>T4: Interfaces and Integration</strong></td>
<td>T4-1 Test structure design &amp; fabrication process toolkit development</td>
<td>T4-2 Integration tech. test structure characterization</td>
<td>T4-3 Flex-v1 design</td>
<td>T4-4 MCM-v1 design</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>T5: Socioeconomic Impact Studies</strong></td>
<td>T5-1 Study environmental impacts of superconductive electronics</td>
<td></td>
<td></td>
<td>T5-2 Study business impacts of superconductive electronics</td>
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Available tools and design flow

- Cell prototype netlist (text file)
- Function simulation (JoSim, JSIM)
- Cell optimization (qCS)
- Layout drawing (Cadence)
- Layout extraction (InductEx)
- Post-layout simulation

Manual design flow

Automated design flow (qPalace)
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Available tools and design flow

qFSIM
ATPG tool for generating tests for delay faults and static faults in RSFQ logic.

qVSim
Post Layout Dynamic Simulation and Verification

qEC
Logical Equivalence Checking Tool For Sequential Circuits

qTV
Timing Verification

qPA
Power Analysis
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Available tools and design flow

FLOOSS: TCAD tool
Inductex:
Layout versus Schematic verification

flooxs.ece.ufl.edu
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Available tools and design flow

**JSIM**
- Time domain solver engine for superconductor circuits developed by T. Van Duzer.
- The models are basic junction models with piecewise linear resistance.
- https://github.com/coldlogix/jsim

**JoSIM**
- Open-source Superconductor Circuit Simulation Engine developed in Stellenbosch university under the COLDFLUX Project.
- Solves netlist based on voltage and phase.
- https://github.com/JoeyDelp/JoSIM

**Other simulators**
- **WRSpice**: SPICE-compatible simulator, written in C++. It offers a fully-featured plotting capability, extensive vector manipulation and post-processing functions.
- **PSCAN2**: comprises a Python module (with accessible source files) and a KLU-library-based linear equation system solver. Include phase space and quasi particle simulation.
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USC Team

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Haolin Cong

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Zeynep Üçpinar

Yasemin Köpür

Neuromorphic Ising machine

VLSI Cell Design

Ising machine

Neuromorphic

DSFQ Ising machine
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VLSI cell design
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Ising Machine

*Wang et al. 2017
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Neural Network

- **Neuron**: Fundamental units of nervous system and brain
- **Soma**: Central cell body acts like a threshold function
- **Axon**: Carries and sends the impulses from one to other neurons
- **Dendrite**: Receives the signals from other cells
- **Axon ending (Axon terminal)**: Forms junctions with other cells
- **Synapse (Neuronal junction)**: The point of contact between neurons

Building on-chip trainable SFQ-based neural network
- Soma with SFQ-based tunable action threshold
- On-chip trainable and scalable synapse
- Axon: JTL & PTL
Thank you

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